Stud Bumping and Die Attach for Expanded

Flip Chip Applications

SUPPORT FOR TODAY'S EMERGING APPLICATIONS

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A good form factor and excellent electrical performance are enabling flip chip bonding to emerge as one of the high growth areas of semiconductor assembly. Growth of this bonding technique will accelerate as substrate prices fall and a manufacturing infrastructure is developed.

Gold stud bumps with gold-gold (Au-Au) interconnect (GGI) have developed as a niche segment of the flip chip market. Gold stud bumping uses a variation of traditional wire bond technology to generate gold bumps on a wafer.[1] After bumping, a wafer is diced and flipped, then thermosonically welded to the gold-plated substrate. Metallurgically, a monometallic thermosonic weld has higher strength and reliability than a solder joint produced by conventional flip chip methods.

Joint development of the stud bump and flip chip die attach process, with optimization of all processes, provides a faster development path than a single party development. These partnerships advance the capabilities of the industry by providing a complete solution.

Advantages of Au Stud Bump and GGI

Two dominant forces control product/process development: cost and functionality. Both solder and plated bumps are wafer-level processes. All bumps are produced simultaneously. Independent of the number of bumps/die, wafer production costs are determined by technology and wafer size (larger wafers are more expensive).

Gold stud bumping is a sequential process, with the bonder producing bumps individually. Depending on the process speed and costs, a high-speed sequential process can be cost advantageous over a fixed-cost batch process. Cost-of-ownership modeling outlines all fixed and amortized production costs, determining the fully loaded costs of a process. Figure 1 compares the costs of different process methods. For low to medium I/O devices, stud bumping has significant cost advantages over electroplated or solder-deposited bumps. As next-generation, higher-speed bonders are introduced to the market, cost of ownership improves, making the stud bump process more attractive to a larger class of products. Figure 1 also shows the crossover points among technologies and how UPH improvements in subsequent generations of stud bump bonders lower the cost to bump a wafer, enabling expansion into new applications.

A cost-of-ownership model for a second-generation platform is shown in Table 1. Costs are grouped in three categories: administrative (labor), capital (installation, shipping, training, depreciation and interest) and variable (capillaries, wire, spares, maintenance, utilities). As bumping speed increases, the cost per thousand bumps decreases from $0.26 to $0.14. Typically, variable costs increase with the number of bumps on a wafer. Administrative and capital costs, however, also rise with the number of bumps on a wafer, because the proportion of machine utilization and fixed costs increase.

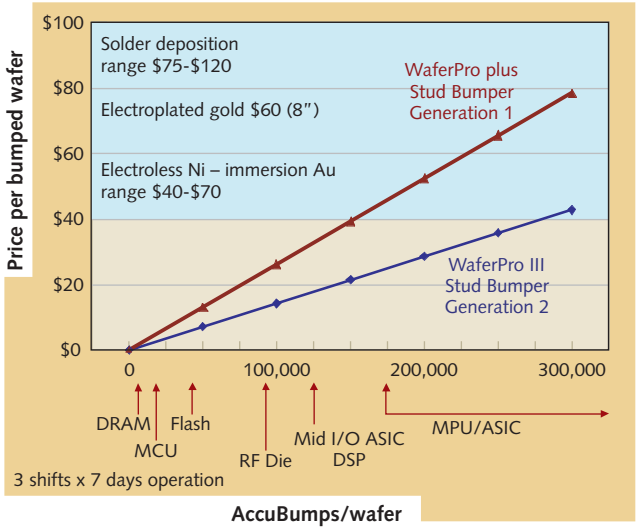


Figure 1. Bumping cost comparison.

The advantages of gold stud bumping and GGI include: lower cost of ownership; infrastructure; flexibility; turnaround time; reliability; higher strength and conductance; no UBM or redistribution layer; and lead-free. In addition to a lower cost of ownership, these partnered technologies demonstrate higher strength and conductance, and a greater flexibility than conventional flip chip methods.

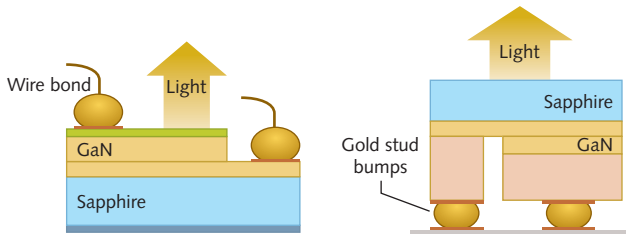


Figure 2. High-brightness LED construction.

Electrical/Material Advantages

The electrical and materials characteristics of stud bump and GGI provide benefits. Gold resistivity is 80 to 85% lower than leaded and lead-free solder alloys, providing better current-carrying capacity.[2] The thermal conductivity of gold is superior to solder, aiding in heat transfer. Unlike solder bumped packaging, stud bump and GGI does not require under bump metallization or an interposer. It's also lead-free.

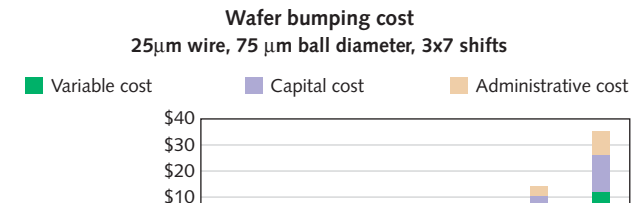
When dice are small and the coefficient of thermal expansion (CTE) is well matched to the substrate, GGI often does not require an underfill. Underfill is an expensive process required for solder flip chip, because solder is prone to fatigue fracture during thermal cycling.

Stud bumping can produce small, inexpensive bumps at 50-µm fine pitch that are inherently taller than plated bumps. Plating processes have difficulty achieving this capability without additional expensive masking operations.

Applications

High brightness light-emitting diodes (HB LEDs) are experiencing significant market growth. Applications for HB LED markets include automotive lighting, LCD display backlighting, signage and general illumination. The $1.8 billion HB LED market from 2002 is expected to grow to $4.7 billion worldwide by 2007.[3] Flip chip attachment plays a key role in delivering the performance to drive this market.

Traditionally, LEDs used wire bond processes (Figure 2). By changing to the flip chip GGI attachment method, several obstacles were overcome. The top wire bond that block light is eliminated. Flip chip contacts replace the inherently thin metal current spreading layers, permitting the device to operate at higher power. In the flip chip configuration, light is projected out the backside of the transparent sapphire substrate to enhance light emission. High thermal conductivity and low electrical resistance of the GGI are superior to solder bump flip chip.



K bumps/wafer	2.5	5	10	25	50	100	250
Administrative cost	0.09	0.19	0.37	0.93	1.87	3.74	9.35
Capital cost	0.14	0.28	0.56	1.40	2.81	5.61	14.04
Variable cost	0.12	0.25	0.49	1.23	2.45	4.91	12.27

Table 1. Stud bump bonder cost-of-ownership model.

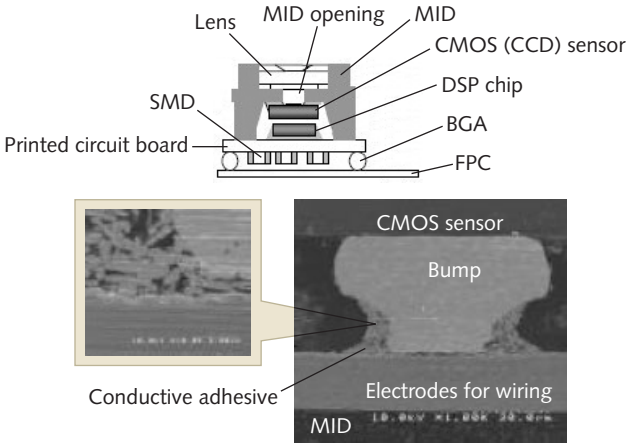


Figure 3. CMOS image sensor construction.

CMOS Image Sensors

Another market segment experiencing growth is the CMOS image sensor. Replacing traditional CCD sensor technology in cell phones and digital cameras, this technology is expected to reach worldwide sales of $4.0 billion by 2007.[4]

The construction of a CMOS image sensor by flip chip GGI is illustrated in Figure 3. Unlike CCDs, CMOS image sensors are produced by standard silicon semiconductor manufacturing processes. CMOS technology enables a chip design that can integrate additional functions such as A/D, clock and digital logic into smaller packages at lower cost. Their lower power consumption makes them attractive for portable electronic devices. With the cell phone substrate area at a premium, a 3-D design* has been developed. A stud-bumped CMOS image sensor chip is bonded to electrodes on the MID substrate with conductive adhesive. Solder reflow temperatures are too high for the MID substrate, so low-temperature gold bonding of stud-bumped die is required. The flexibility of the stud bump and flip chip attach process allows applications that, otherwise, could not be manufactured.

Flip Chip Bonders

The migration from previous 3-mm², low I/O SAW filters and oscillator devices into new generation 5- to 10-mm², medium I/O applications is shown in Figure 4. The new, higher I/O and larger applications require greater force and increased ultrasonic energy, which are available in newer generations of flip chip bonders. New tool configurations are also improving coplanarity between the substrate and the tool, ensuring uniform distribution of the bond force and ultrasonic energy for uniform bond strength. Older-generation equipment is unable to achieve the uniform bond strength required of today's high-reliability devices. A comparison of new-generation flip chip bonders with previous generations is shown in Table 2.

	Machine generation		
	G1	G2	G3
UPH	650	2000	3600
Cost Improvement*	100	20	8.4
Accuracy	+-15mm	+-15mm	+-10mm
Max. Die size	4x4mm	5x5mm	10x10mm

*Based on (machine cost)/(UPH/ m" floorspace)
Assuming a value of 100 for Generation 1 machine, G2 and G3 Cost Improvement values show relative cost reductions due to speed improvements and floorspace reductions.

Table 2. GGI flip chip bonder capabilities.

Conclusion

Flip chip bonding is predicted to grow at a compound annual growth rate of 27% through 2008, increasing from 4.5% of the total current wafer production (200-mm equivalent) to 12% in 2008.[5] The latest processes for flip chip bonding and newer generations of stud bump and flip chip equipment provide a compelling cost of ownership for this technology.

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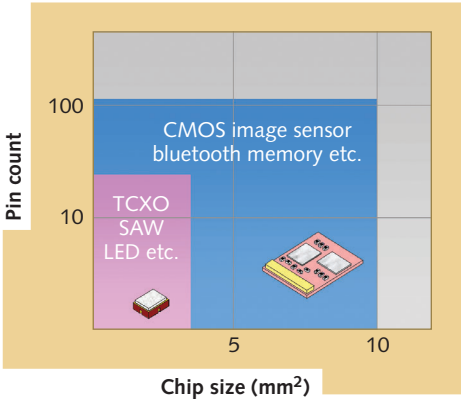

Figure 4. GGI market growth.

References

1. L. Levine, "Ball Bumping and Coining Operations for TAB and Flip Chip" Proc. 1997 ECTC.
2. Siewert, Liu, Smith, and Juan Carlos Madeni, "Properties of Lead-free Solders Release 3.0," NIST and the Colorado School of Mines, May 31, 2001.
3. "LED Market Report from Strategies Unlimited," Product Release. July 15, 2003.
4. "Image Sensor Market at a Critical Point, Says Strategies Unlimited," Press Release. October 1, 2003.
5. "Neil Moskowitz, private communication," Prismark Partners LLC, 130 Main Street, Cold Spring Harbor, NY 11724.

*Molded Interconnect Device (MID).

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