Probing wire bond issues for bonding over Cu/low-K dielectric materials

Bob Chylak , Frank Keller, Lee Levine, *Kulicke & Soffa Industries Inc., Willow Grove, Pennsylvania*

OVERVIEW: The introduction of low-k and ultralow-k dielectric films in copper-interconnect structures presents serious challenges in test, assembly, and packaging of advanced devices. Low-k films support higher circuit speeds and enable smaller feature sizes by increasing the insulation capability around copper interconnects, but compared to previous generations of silicon-dioxide dielectric layers, the new materials have substantially weaker mechanical properties and reduced thermal conductivity. Fragile low-k materials increase the risk of damage to finished devices in wafer probe test and high-speed final assembly processes. Compounding the situation is the simultaneous introduction of copper interconnects and ultra-fine pitch pad layouts. Experiments on wafer designs with different pad structures have been conducted to determine optimal structures and other factors for improved process robustness in probe test and wire bonding.

--

As 90nm technology ramps into volume production and R&D efforts target the launch of 65nm wafer processes in 2007, the need for copper metallization, combined with the use of low-k dielectric layers, becomes a critical challenge in all phases of semiconductor manufacturing, but especially in final assembly plants. Previous process generations, using silicon-dioxide (SiO_2) insulators in interconnects (with a dielectric constant k = 4.2), represent the standard against which new processes are compared. Because of its high strength and fracture toughness, SiO_2 provides ease of manufacturing.

Unfortunately, every low-k material in development has significantly reduced fracture toughness. Replacing SiO_2 with a lower k dielectric requires utilization of fragile materials with substantially weaker mechanical properties and reduced thermal conductivity. High-speed, demanding semiconductor assembly processes, wafer probe, and wire bonding generate significant stress levels. The use of copper interconnects and ultra-fine pitch pad layouts also add complications in test and final assembly.

To contrast the design of pad structures and analyze tradeoffs in packaging materials and processes, designed experiments (DOEs) were conducted with 10 separate wafer designs. The DOEs demonstrated significant differences in bondability. The experiments involved the two main types of low-k dielectric materials: chemical vapor deposited (CVD) inorganic films and spun-on polymer organic films.

Optimally designed structures provided significantly better process robustness. Analysis using Focused Ion Beam (FIB) for cross-sectioning the die after wire pull and ball shear testing demonstrated the absence of hidden mechanical failures. Results from wafer probe tests and tradeoffs and optimizations for capillary and wire materials were also covered in the DOEs.

Low-k's growing momentum

IC performance and cost propelled the development of low-k dielectrics in wafer processing. New low-k materials offer increased insulating capability which, when combined with copper technology, enable higher speed circuitry (improved performance). With copper and low-k interconnects, costs can be optimized by packing more circuitry on a die with finer lines and reduced feature sizes. Additionally, fine-feature technology creates die sizes that require more input/output contacts than permitted with a normal peripheral I/O design layout, often referred to as pad-limited

designs. Wire bonding over active circuitry on copper/low-k metallization layers is often required for these designs because it improves utilization of available silicon real estate.

As chipmakers race to market with products built using next-generation process technology, lowering the dielectric constant between the interconnect layers becomes necessary. In the past year, initial production of 90nm technology and low-k ICs began at a number of device manufacturers. Low-k is generally defined as k value of less than 3.0, which can be reached with inorganic, organic, or hybrid films. They are deposited by CVD or by spin coating the wafer. Fluorinated silicon glass (FSG), a widely used material in some 130nm processes, offers a k factor of 3.6, which is not considered "low k." There are two competing process technologies: CVD carbon-doped oxides (SiOC) and the organic spun on polymer dielectrics[3]. Applied Materials Inc.'s Black Diamond is an example of the former and Dow Chemical Co.'s SiLK is an example of the latter.

Key advantages of the polymers include its extensibility, good dielectric characteristics, and proven well-characterized materials. The dielectric constant of commonly used polymers ranges from k = 2.5 to 2.8. The main challenges of polymers include lower mechanical properties than oxide, reduced thermal stability and conductivity than oxide, and potential out gassing with higher gas permeation[3].

The carbon-doped oxides fit well into normal wafer-fabrication process flows and have better hardness, elastic modulus, thermal conductivity, and lower coefficient of thermal expansion (CTE) than polymers. However, they are not considered to be as extensible as the spin-on dielectrics (SOD). Applied's Black Diamond SiOC has k = 2.8. Air has a k value of 1.0. Therefore, to further reduce the k value of films, a material's porosity must be increased. Increasing porosity, however, will further degrade the mechanical properties.

Recent developments have been made in the hybrid area. Many customers are going forward with hybrid integration schemes that employ both polymers and carbon-doped oxides. The hybrid approach is complimentary as the polymers help protect the carbon oxide materials from via poisoning and etch damage, while the oxide materials provide added strength to the dielectric stack in the hybrid composite structure.

Assembly challenges with low-k

The primary goal of backend manufacturing processes is to assure device reliability; therefore, preserving the integrity of the complex stack of dielectrics and metals from the silicon circuitry to the bond pad is essential.

Mechanical strength and thermal compatibility are critical parameters for successful integration of low-k dielectrics in multi-level Cu interconnects. During the life of the device, mismatched CTE transmits strain to the weaker material, which may fail prematurely. Hardness and elastic modulus are good indicators of whether a material can survive test, wire bond, and packaging processes, and provide good long-term reliability. Table 1 shows the mechanical properties of SiO_2 and the common low-k dielectrics. The large differences in elastic modulus and CTE show the significant challenges presented by low-k dielectrics. New techniques, specially configured equipment, and optimized process development are required to successfully achieve the levels of manufacturability that the industry demands.

Table 1: Low K material properties [2]

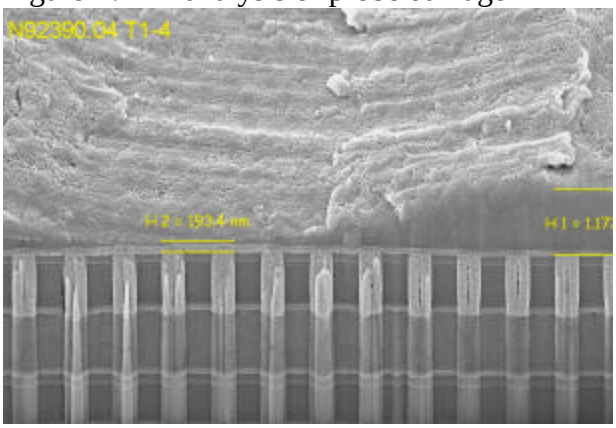
	SiO2	SiOC	Organic Polymer
Hardness (Gpa)	9.0	2.0	0.38
Elastic Modulus (Gpa)	80.0	10.0	0.3
CTE (ppm/deg C)	0.5	12	62

Most low-k dielectrics are soft and spongy, with the polymers even more so than the CVD materials. During wire bonding, both the wire (ball or wedge) and the bond pad deform together, forming the bond. The soft, spongy layers within the structure allow the top metallization layer to cup and deflect under the ball, preventing the co-deformation necessary for bond formation[2]. FEM modeling, stiffening structures, and wafer design optimization will help to define and overcome the problem. In DOEs, it was found that optimized wafer design had a significant effect on wire bonding process robustness. Optimized designs had a much larger "bond window," which is defined as the region where defect-free bonding could occur. Other designs, with different via structures or underlying layers, had significantly fewer defect-free cells and were more susceptible to peeling and pad damage.

It was found that spin-on materials are more susceptible to cracking, and the organic material within them may contaminate the interconnection, leading to degradation. Silicon foundries have acknowledged that problems with spin-on materials, such as thermal stability and mechanical strength, will be "major challenges" as the technology advances. But, many believe that neither spin-on nor CVD low-k dielectric materials truly satisfy all of the electrical, chemical, mechanical and thermal requirements and that integrated combinations of the two will be necessary.

Wafer probe optimization

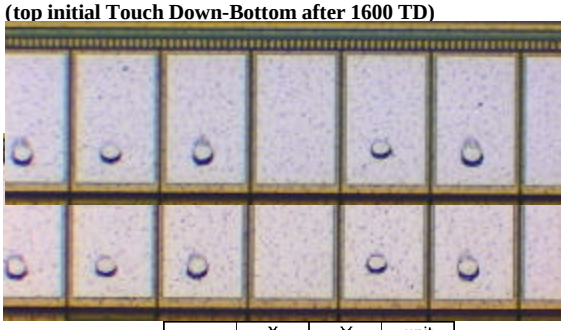
Figure 1: FIB analysis of probe damage



Work was done to quantify the size of the probe tip damage to pads to determine whether minimizing it would improve bondability. Figure 1 shows an example of the damage that occurred on a probed bond pad. Minimizing this damage is an important goal.

A new type of radiused tip wafer probe pin with a lower force-per-displacement has been developed and tested. This design, used on a new card called K&S DuraPlus, creates smaller and more accurate probe marks. Figure 2 shows photos of probe marks from the new pin after

Figure 2 DuraPlus Ô Probe Data
(top initial Touch Down-Bottom after 1600 TD)

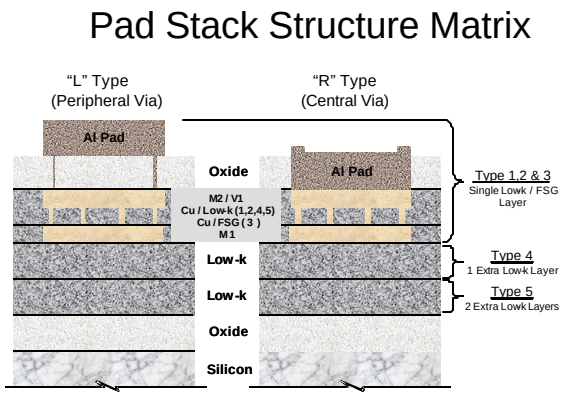


	X	Y	unit
first die	12.5	18	um
last die	12	19.5	um

the first cycle and 1,600 cycles later. Measurement of the probe mark demonstrates that they have maintained their size and consistency. The pin can maintain probe marks within a 25-by-30µm area and exerts only 1.5 grams per mil of over-travel. It is well suited for rectangular pad designs that separate probe marks from the bond area, or for staggered, tri-, or quad-tiered designs that may have bonds over active circuitry (BOAC). Low-k dielectric applications are now under test.

Pooling resources for DOEs

Figure 3. Basic 2 level Cu-low K film stack, (L) with passivation directly under Al pad, (R) no passivation under Al pad



Combining resources and specialists, K&S collected data from 10 wafer designs as part of a multi-company collaboration[4]. These wafers were produced and bonded with metallization described in Figure 3. The five wafers, shown as the "L type," in the figure, had peripheral vias and passivation directly under the bond pad. The "R type" wafers had a central via. Types 1 & 2 wafers had slightly different low-k/Cu metal directly below the pad. Type 3 wafers had a FSG glass dielectric. Type 4 had two low-k/Cu metal layers (1 extra) and Type 5 had three low-k/Cu metal layers (2 extra). The same 16-cell ECHIP DOE (based on software from ECHIP Inc.) was run on all 10 wafer combinations.

Contrasts analysis was used to determine the statistical significance of structural differences in the wafers on robustness of the wire bonding process. Figure 4 shows a summary of the number of cells in each 16-cell DOE that had no failures. It's clear that the L column, peripheral via, was the best structure, based on the results. The FSG glass dielectric Type 3 significantly outperformed the low-k dielectric treatments. Although FSG glass is not a low-k dielectric, the combination of Cu and FSG provides good

Figure 4. Number of zero-failure wirebond DOE cells (out of a total of 16 cells) for each film stack

Peeling Summary per Pad Type

Lower Structure Type	Upper Structure Type L	Upper Structure Type R
1	1	0
2	9	0
3	16	16
4	3	0
5	6	0

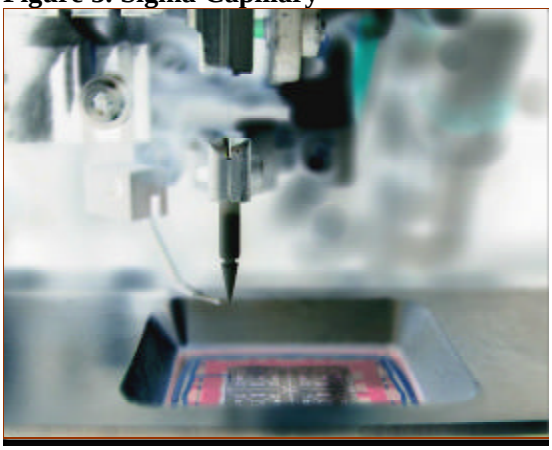
- Chart indicates number of experimental cells (of 16) for each pad structure where no peeling occurred
- Process window is proportional to number of cells with zero pad peeling failures

performance and should be considered for designs where its performance is acceptable based on its excellent manufacturability.

One other unexpected effect was that additional layers of dielectric/metal actually improved performance (treatments 4 and 5). FEM analysis later confirmed these results and explained that the additional layers shared the load and resulted in reduced plane strain. Subsequent work using FIB analysis of structures with metal lift and peeling determined that, in many cases, the defects observed after pull testing were not present in the as-bonded samples and were artifacts of pull testing. Pull testing small diameter ball bonds must be critically controlled and understood, otherwise invalid conclusions can be reached. As ball bond pitch moves below 40µm it is likely that the pull test will become less important and that shear strength will be considered the only valid measurement technique[5].

Materials Optimizations

Figure 5. Sigma Capillary



It has been shown experimentally that optimization of the capillary and wire is beneficial for low-k and pad-sensitive applications, such as BOAC. A new capillary design, called "Sigma", demonstrated improved process robustness with sensitive materials when compared to a standard cap. Ultrasonic transducers, even though they are designed to vibrate in the Y direction, actually generate displacement in the X, Y and Z directions. This is a result of small asymmetries and manufacturing tolerances. In the Sigma design, a ring is cut in the upper potion of the capillary, which increases the movement at the tip of the cap but with less vibration. This isolates and eliminates the Z displacement, while amplifying only the Y component of the ultrasonic amplitude. As a result, less Z strain is generated within the pad structure. Figure 5 shows the Sigma capillary design.

Wire developments for low-k and ultra-fine pitch devices have focused on 4-9's wire alloys (99.99% Au). These alloys exhibit improved long-term reliability, stronger and stiffer mechanical properties (as wire diameter is smaller than in the past). They also exhibit excellent ball formation properties for bonding on small bond pads[6].

Conclusions

Assembly of Cu-Low dielectric devices represents a new challenge to back-end semiconductor manufacturing. All of the critical manufacturing processes must work together with front-end design functions to develop robust designs and processes that meet the exacting yield and productivity standards that the industry has established. Wire bonding will meet the required challenges. New machines and controls, such as the K&S Maxum *plus*, which are capable of achieving the low impact, low stress requirements of low K materials, will be required for this task. Specially tuned ultrasonic transducer and capillary combinations, such as the Sigma capillary, will enable high strength bonding without generating the Z axis strains that damage delicate chip structures. High reliability wire alloys, such as the AW-66, will produce ultra-fine pitch bonds with excellent long-term reliability.

References

1. Meggy Gotuaco, Peter W. Lee, Li-Qun Xia, Ellie Yieh, "The Case for CVD Low K", Volume 1, Issue one, Applied Materials Update 2002.
2. Lee Levine, "The trend toward copper with low k layers continues", Chip Scale Review Jan-Feb. 2002.
3. Donald C. Frye PhD, "Packaging Challenges for Advanced Low K for Flip Chip and Wire Bond", Ninth Annual K&S Semicon West Technology Symposium, July 2002.
4. Jon Brunner, Frank Keller, Tony Pan, "Optimization of Wire Bonding Over Cu-Low K Pad Stack", Proceedings of IMAPS, November 2003, pg
5. V. Sundararamen, D.R. Edwards, W.E. Subido, H.R. Test, "Wire Pull on Fine Pitch Pads: An Obsolete Test for First Bond Integrity". Proceedings ECTC 2000
6. Inderjit Singh, Lee Levine, Jon Brunner, "Reliability Ground Rules Change at <50µm Pitch", Proceedings IEMT 2003

Bob Chylak holds a dBSEE degree from Penn State University. He holds two patents. Chylak is vice president of packaging and process integration for Kulicke & Soffa Industries Incorporated, 2101 Blair Mill Road, Willow Grove, PA 19090; ph 215/784-XXXX, fax 215/784-XXXX, e-mai bchylak@kns.com.

Frank Keller holds a MS degree in Industrial Engineering from Penn State University and a BSEE from Spring Garden College. He also holds a B.S. in Business Administration from Penn State University. Keller is manager of process R&D at Kulicke & Soffa.

Lee Levine received a bachelor's degree in metallurgy and materials science engineering from Lehigh University in Bethlehem, PA. He received the John A. Wagnon Technical

Achievement Award from the International Microelectronics and Packaging Society. Levine has been granted four patents and is a senior member of the technical staff for Kulicke & Soffa's Advanced Packaging Ball Bonder Division.