New Trends in Wire Bond Packaging

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As new high-speed products with ever increasing capabilities are developed and introduced into the market, new advanced IC packaging designs and methods also must be developed to meet these new products' requirements. New advanced packages are being designed to maximize I/O numbers, minimize wire bond loop length, and provide System-In-a-Package (SiP) performance. Stacked die packages, providing (SiP) performance, are already the mainstream of cellular phone manufacturing. Wire bonded Lead-On-Chip (LOC, FBGA) packages are the largest production volume portion of the DDR I memory market, and will be the dominant package type through the DDR II generation[1].

Even with changes in package design, wire bonding continues as the preferred interconnection method because of its' low cost, flexibility, reliability and established infrastructure. In the FBGA package, wire bonded interconnects have demonstrated excellent high-speed electrical performance. The FBGA design utilizes short wire lengths and centrally located interconnections that achieve the required on-chip timing.

Area array bonding, with three and four tiers of bond pads, can provide the highest I/O capability and still maintain large wire diameters for mechanical and electrical performance. QFN packages use leadframe and molding materials efficiently, providing low cost and high yield for high volume, low pin count surface mount packages. In today's constantly changing production assembly environment where engineering changes, die shrinks, small lots, and fast changeovers occur daily, wire bonding still provides the flexibility to meet the needs of high volume assembly.

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Machine Requirements and Trends for Advanced Packaging

The new advanced package designs place significant new demands on assembly machines and processes which, in many cases, can only be addressed with the latest generation of wire bonding machines - with upgrades tailored for the new packages. For example, many of the new BGA packages have more than 800 I/Os and are designed with bond pads of 40 μm pitch.

Some of the new machine requirements for wire bonding these ultra fine-pitch packages include:

- Improved bond placement accuracy (+/-2.5 μm).
- Enhanced Electronic Ball Control (EBC).

- Improved Z-axis force and position control for greater loop shape repeatability.
- Higher bond speed (approximately 16 wires/second for a standard shape, 2.5mm length loop) for improved productivity with high I/O devices.
- Vision engine improvements that offer greater recognition accuracy and speed.

These new machine capabilities enable the formation of loop shapes that were previously unachievable. Improvements to Z-axis force control also provides accurate, real-time force tracking during the bonding of stacked thin cantilever die that may be resonating. The Kulicke & Soffa Maxum™, bonder (see photo 1) with 40μm pitch is an example of an out-of-the-box, next generation wire bonder that offers these capabilities. The greater loop shape capabilities, enhanced motion controls, higher speed and process flexibility of K&S' Maxum and other new wiring bonding machines also help increase manufacturing productivity and profits in today's fast paced, ever-changing assembly facility.

New Loop Shape Capabilities

The proliferation of new advanced IC packages continues to drive the creation of interesting new wire bonding loops shapes. Figure 1 displays examples of a few of the many possible loop shapes that can be produced by current generation wire bonders. Only a few years ago, it seems that standard 10 mil high loops were the only choice available in wire bonding. Then, low (5-6 mil) loops were developed for TSOP (Thin Small Outline Package) packaging.

TSOP loops demanded improved machine control capabilities, both in wire feed and machine movement controls. The "worked" or trapezoidal-shaped loop was soon required for memory devices. As these devices had internal bond pads, they needed a long flat length parallel to the die surface that was provided by the worked loop shape. The worked loop is also more reliable in applications that undergo thermal cycling as it can better withstand the differential motion caused by a thermal expansion mismatch than a standard loop shape. During the cycles of expansion and contraction, it flexes at the middle kink, rather than in the HAZ above the ball where fatigue cracks are more likely to form[2].

Chip Scale Package (CSP) loops are a variation of the worked loop. Stand-off-Stitch Bumps (SSB), along with reverse bonding (ball on substrate, stitch on SSB), are often required for stacked die applications, especially for the highest positioned die in the stack. This combination provides for the lowest bond height capability, while minimizing the total package height. SSB bumps can also be used as a single bump or in stacked bump combinations for low-cost, flip chip applications. In flip chip applications, the bumps are attached to the substrate through thermosonic bonding, with anisotropic conductive or non-conductive adhesives.

Lead-on Chip Packages for High-Speed Interconnect

Current generation memory devices are predominantly wire bonded. As memory transitions from TSOP to FBGA (DDR I & II) package designs, wire bonding will continue as the highest volume interconnection method. Wire bonded FBGA packages have proven to meet the electrical performance requirements for both DDR I and DDR II memory up to the PC5400 generation of DDRII (chip speed of 667MHz, bus speed 400 MHz). FBGA packages are designed with short wire loop lengths that have low inductance and are capable of the high speed switching required by fast memory. New variations of the FBGA package may further improve electrical performance and move wire bonding capabilities into even higher speed packages where the low cost of wire bonding provides a competitive advantage.

Stacked Packages Go Mainstream

Within the past several years, stacked die packages have moved into high volume production as they offer a SiP solution for many applications. Figure 2 shows a collage of stacked die looping photos. To provide the interconnection between the layers, stacked die packages require a variety of loop shapes within the same package. Bottom layers often require CSP loops, with a second bond located very close to the die edge. Upper layers require reverse bonding, with a second bond placed on a stand-off-stitch bump. Bonding to thin cantilever die (as thin as 0.1mm) is another challenge posed by stacked die looping. Thin dice attenuate ultrasonic energy as they bend and flex during bonding. Active force control is required to provide good bonding to surfaces that are dynamically bending and bouncing[3].

Area Array Packaging Creates New Era in Wire Bonding

The advent of massive area array wire bonding has created a new era in wire bonding. New packages with three tiers of wire bonds are in production, with four-tier packages entering the qualification process. Figure 3 shows four-tier loops on a mirror test die. Area array wire bonding competes with the high I/O capabilities of flip chip. A four-tiered area array device with 60μm pitch has an effective pitch equivalent to a 15μm pitch peripheral design, yet has the larger ball bonds and larger wire diameter associated with a 60 μm process.

Qualifications of test structures with 3 and 4 rows of staggered bond pads will be completed this year. Among the advantages of area array wire bonding include its relaxed pitch requirements and use of 1 mil wire. One mil wire is the standard in semiconductor manufacturing as it has greater strength and superior electrical performance than smaller diameter wire. The mechanical and electrical performance of smaller diameter wire falls off significantly relative to 1 mil wire. For example, the strength of a 0.7mil diameter wire falls by 51% and stiffness

(resistance to deflection) by 76 %, while its' electrical resistance more than doubles. Area array wire bonding offers significant advantages in mechanical and electrical performance. And because it provides a cost-effective solution for advanced packaging, its usage will grow rapidly.

QFNs Prove Cost Effective

QFN (Quad, Flat, No-Lead) packages are a high growth segment of the market because of their excellent cost performance. By using a matrix leadframe (See Figure 4) containing many device sites in each index window, processing efficiency is improved. Wire bonding and die attach throughput significantly increase through reduced materials handling time. QFNs use a less complex and less expensive pancake mold cavity, so that all of the devices in each index window are encapsulated within the same large mold cavity. This configuration results in reduced molding costs and significant materials savings. After molding, the devices are singulated with a wafer saw and the exposed leads are prepared for surface mount assembly. New high-speed equipment, such as the K&S Nutek™,, can often replace older generations of manufacturing equipment in this application. Replacing older machines at a ratio of approximately 3:1, new machines significantly improve cost of ownership and reduce required footprint.

New Bonding Tool Capabilities and Requirements

As the pad pitch of leading-edge devices has decreased, so have the size and tolerances of the tool features that control bonding. Atlas™ is a new generation ceramic material with finer grain size and higher fracture toughness developed specifically for ultra-fine pitch applications. In addition to improving capillary polish (polished surfaces reduce build-up of contamination during bonding, a major source of capillary degradation), Atlas offers a higher fracture toughness that reduces the incidence of capillary tip fractures in ultra-fine pitch and bottleneck capillaries with wall thin cross sections (often less than 25μm) between the capillary hole and outside cone.

Recently introduced into the market, the Sigma capillary (Photo 2) represents a significant change in capillary design. The result of extensive FEM modeling and laser vibrometer testing, the Sigma capillary improves bond strength while allowing the use of a lower ultrasonic energy input. Equivalent standard designs cannot offer this. The Sigma's lower ultrasonic energy input proves advantageous when bonding the delicate low-K dielectric pad structures that are required for state-of-the-art ICs.

As dielectric constant K decreases, modulus and strength also decrease, resulting in bonding difficulty and yield loss. Sigma capillaries help reduce this yield loss and provide defect-free bonding of low K devices. In addition, the Sigma design allows the use of a slightly larger wire diameter than was previously possible for an equivalent bond pad pitch. Increased wire diameter

provides better mechanical performance (strength and stiffness) for improved looping and molding in packages with long wires. Larger wire diameter also possess a higher electrical conductance. Conductance decreases significantly as diameter decreases in ultra-fine pitch wire bonds.

New Bonding Wires for Advanced Packaging

New package designs also place increased demands on bonding wire. New formulations of 99.99% Au wire address these demands. As ball bond pitch decreases, wire diameter must also decrease. Producing small diameter ball bonds requires wire with mechanical properties tuned to meet the demands of the process. For a high yield process, low loop, small and spherical balls must be uniformly formed at high speeds (accelerations of > 25g). New wire formulations, therefore, require higher strength and stiffness than were previously necessary. Intermetallic weld formation and properties also must be controlled to provide good long-term product reliability. The AW-99 and AW-66 wires, from Kulicke & Soffa, are examples of new bonding wire developed that meet these specific requirements.

Conclusions

Because of the high degree of flexibility offered by the wire bonding process, the industry will continue to develop new, innovative wire bondable package designs. Easy changeovers, user-friendly program adjustments and lower manufacturing costs continue to make wire bonding the process of choice for many IC package designs. New bonding machines, such as the Kulicke & Soffa's Maxum IC Ball Bonder, provide the high speed, superior accuracy and controlled looping capabilities that are required for profitable manufacturing.

The new tool designs and improved strength and fracture toughness of bonding capillaries, such as those offered by MicroSwiss, provide longer life and high product yield for greater profitability. In addition, the high reliability and strength of new bonding wire provides the high quality, reliable intermetallic bonding that is required for many new ultra-fine pitch devices. By combining the capabilities of the newest bonding machines, tools and materials in one integrated process, more robust solutions can be developed that address a variety of today's demanding process needs than can be found through a single-source supplier.

[1] S. J. Pan, et. al., "A Comparison of Electrical Performance between a Wire Bonded and a Flip Chip CSP Package", Proceedings Semicon West 2003
[2] P. Hoffman, et.al., "Development of a High Performance TQFP Package," 1994 Electronic Components and Technology Conference, pp 57-62

[3] R. Chylak, I.W. Qin, “Packaging Challenges and Solutions for Multi-Stack Die Applications,” Proceedings IEMT 2001