Look for Wafer-Level Packaging to Rule as the Natural Choice for Opto Packages

By Lee Levine, Contributing Editor

Within the past several years, wafer-level packaging (WLP) has emerged as an attractive solution for chip-scale packaging because of form factor and cost attributes.

Consider that the WLP footprint is the same as the chip, and offers the possible smallest form factor of 1:1. WLP is completely assembled on the wafer prior to dicing, with an assembly that includes all solder bumps, passivation and polymer layers. Additionally, and unlike flip-chip processing, WLP employs only standard surface mount assembly for substrate connection.

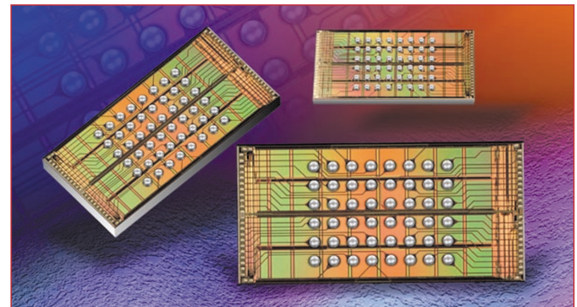
Also, wafer-level packaging shares the cost advantages of both full wafer processing methods and standard SMT assembly processes. Further cost advantages inure to WLP because it is invariably accomplished in batch mode, rather than by individual die.

IPDs at the Wafer Level

WLP is currently employed in volume production for integrated passive devices (IPDs), serial E^2PROMs and analog and power (handheld) devices. In the future, WLP will be a natural choice for optoelectronic packages, because WLP fits well within the opto manufacturing sequence.

Opto device assembly requires precise surface mount assembly and reflow soldering, as does WLP. In addition, opto packaging often employs LTCC substrates. Wafer-level-packaged parts can be attached to LTCC without the constraints of other substrate materials, where large TCE mismatches cause reliability problems.

The TCE mismatch between ceramic substrates and silicon flip-chipped devices is small enough that WLP used with ceramic seldom requires an underfill for reliability.



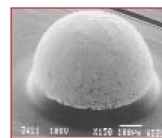


Illustration shows a WLP with a close-up view of the Polymer Collar that constrains the bump and improves thermal cycling life, reportedly by better than 50 percent.

Solder-Joint Fatigue

In any solder-attached assembly operation, solder-joint fatigue, as demonstrated by thermal cycle testing, represents the most significant long-term reliability risk. Chips with larger distance from the neutral point (DNP), which is the distance from the center of the farthest bump, will present more difficulty withstanding fatigue.

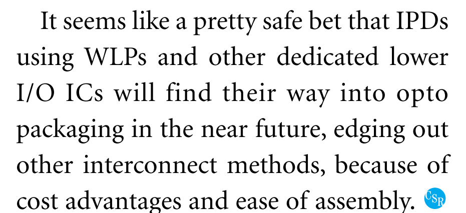
The introduction of the WLP with Polymer Collar (a polymer layer that is applied to the wafer and wicks up the edge of the ball, providing a constraint) by Kulicke & Soffa's Flip Chip Division has been shown to improve reliability. It has also demonstrated a 50-60 percent increase in thermal cycle testing on FR-4 substrates.

WLP, employing an FR-4 substrate, represents the worst case combination, because the TCE of FR-4 (15 ppm/C°) is significantly higher than Si (2.2 ppm/C°). The TCE differential causes strain in the solder interconnects during thermal cycling. The addition of the Polymer Collar changes the dominant failure mode from cracking at the interface of the intermetallic layer to cracking through the bulk solder—a major accomplishment.

Changing the failure location from the brittle intermetallic interface and into the bulk solder signifies that the best achievable properties for the solder alloy have been attained.

Most cell-phone makers specify a board-level thermal cycling requirement of 300-800 cycles with a temperature range from -40°C to 125°C. WLP testing conducted by the K&S Flip Chip Division demonstrated more than 1500 cycles with a 6.8 mm (4.88 DNP) die size.

It seems like a pretty safe bet that IPDs using WLPs and other dedicated lower I/O ICs will find their way into opto packaging in the near future, edging out other interconnect methods, because of cost advantages and ease of assembly.



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