Development of 100+ GHz High-frequency MicroCoax Wire Bonds

Sean S. Cahill[#], Eric A. Sanjuan[#], and Lee Levine*

[#] BridgeWave Communications, Inc.
3350 Thomas Rd.
Santa Clara, CA 95054
PH: 408-567-6900 Fax: 408-567-0775
Email: seanc@bridgewave.com www.bridgewave.com

* Kulicke & Soffa Industries, Inc.
1005 Virginia Drive
Ft. Washington, PA 19034
PH: 215-784-6036 Fax: 215-784-6014

Abstract

Wire bonding is today's leading IC interconnect technology, comprising over 90% of all interconnects. As device operating frequency increases, however, customers look to other interconnection methods, including flip-chip, to provide better signal transmission properties for higher volume applications. Ribbon bond, mesh-bond, and, ultimately, machined waveguide are utilized for lower volume applications. Other next-generation approaches, such as wireless or optical interconnect, are garnering increasing research dollars, but are, in practicality, many years away. These approaches are considerably more expensive and less flexible than wire bonding, either because of tooling costs, or added labor-intensive steps. Flip-chip is limited as an approach because it does not address cross-talk issues without requiring numerous extra bumps for shielding. This paper describes a new interconnect approach called, MicroCoax, that is based upon wire bonding, and has the capability to create high-bandwidth interconnects for increasingly higher frequency electronics. Using this approach, prototype devices were designed and fabricated demonstrating excellent performance over DC-100+ GHz frequency range. Transmission line losses were less than 0.5 dB for a typical 2 mm long wire bond on 160 µm pitch, and cross-talk isolation was 40-50 dB from DC-50 GHz. Applicable to printed circuit boards and device-level interconnects, MicroCoax technology allows data signals to flow over large frequency ranges with excellent impedance match and little cross-talk. Its fabrication uses existing infrastructure within the microelectronics arena, allowing for easy adoption.

Key words: High-frequency, GHz, interconnect, coax, bandwidth, wire bond

1.0 Introduction

In 1965, Gordon Moore, co-founder of Intel, made the empirical observation that at our rate of technological development, the complexity of integrated circuits will double in about 24 months. This observation is now known as Moore's Law.[1] By 2001, Intel was offering processors operating at 3.8 GHz with plans to scale up to 10 GHz. Unfortunately, at these frequencies, simple unshielded wires in today's interconnects begin to look less like pipes routing information, and more and more like antennas diffusively broadcasting loudly to all their neighbors. While simple wires interconnecting chips address about 95% of today's chip "packaging" needs, these simple interconnects are, increasingly, being recognized as limiting chip and system performances.

In addition, wireless communications are transitioning to 10's of GHz for more bandwidth, with automotive anti-collision radar systems operating near 80 GHz. When electronic systems run at these speeds, they too suffer severe component-to-component interconnect performance limitations because simple unshielded wire interconnects are no longer able to provide the needed interconnections *between* components.

Flip-chip approaches are not a panacea, as these mostly unshielded structures tend to stall in performance at frequencies approaching 20 GHz due to cross-talk, a draw back involving nearest neighbors "leaking" signals to one another. The denser the number of flip-chip bumps (talkers), the worse the cross-talk. Significant initial tooling costs for each and every design is another drawback for flip chip processing. One small design change has major impacts on chip packaging costs. Therefore, flip-chip is economically viable primarily for very large volume, large I/O count, static designs. Companies have been willing to invest in flip-chip approaches, despite their expense, because there is clearly a need for improved performance.

Although chips are getting faster and denser, their ability to retrieve and store data from external sources is not increasing as quickly. As a result, the rate of improvement in the performance of key computing tasks, such as simulation, signal processing and database searches, is becoming limited by off-chip bandwidth. Some argue that this could drive computing off the 40-year performance advancement curve derived from the Moore's Law improvement in semiconductor technology.[2] A solution must be found. The good news is that if one is found, it should bring benefits in terms of I/O density, cost, speed, latency and power consumption.

2.0 MicroCoax Approach

MicroCoax, an approach based on wire bonding, is similar in structure to common 50Ω coax cable. MicroCoax should allow data signals to flow over large frequency ranges from 0 to 120 GHz, with significant impedance matching and little cross-talk, from one location to another on a chip, and from chip-to-chip in a system. The main difference between MicroCoax and common coax cable relates coax sizes, connectivity, and fabrication.

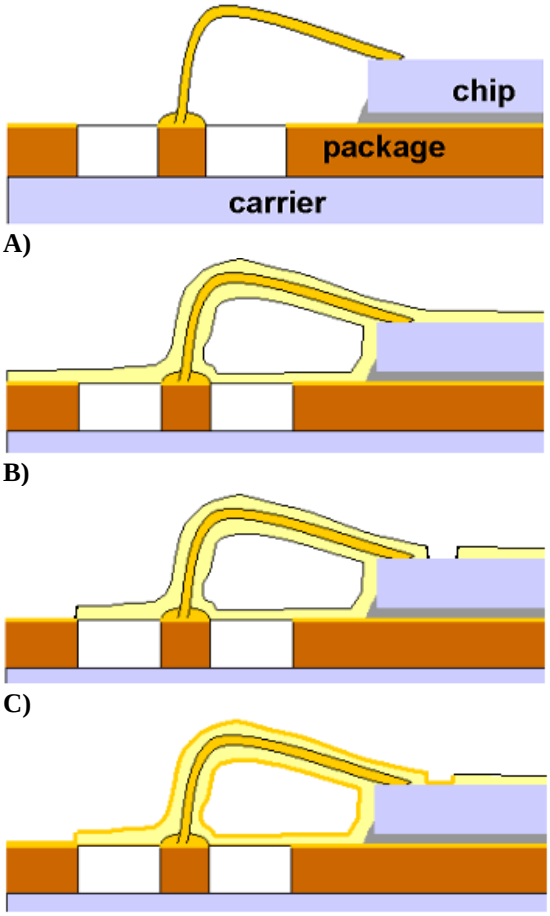

Figure 1, A-D: MicroCoax Process Sequence

A typical MicroCoax is about 80 microns in diameter, or about the width of a single human hair. Figure 1 illustrates the procedure for fabricating MicroCoax. First, a semiconductor chip is attached to a package or board. Then, the chip is wirebonded (Figure 1-A) using a conventional wire bonder, such as a Kulicke&Soffa (K&S) model. Next, the chip and wire bonds are coated with a plastic layer that is very uniform, and with a thickness determined by desired electrical characteristics, such as impedance (Figure 1-B). This layer is known as the coax dielectric. The metal on the outside of a coax is ground, such as with MicroCoax. Small holes are made, using standard laser trimming equipment, in precise locations on the package and the chip (Figure 1-C) to connect the outside metal to ground. Figure 1-D shows that the ground metal layer is then deposited onto the chip/wirebond/dielectric assembly, and selectively patterned (so that ground metal is not on the chip surface), using a simple lithography step.

The electrical ground on the outside of the cable shields coax cables from noise and prevents signal leakage. Unlike bare wires or flip-chip bumps, coax cables are matched in impedance to the devices that they connect. This means that signals get out of and into the connected devices, without needless bouncing around inside the cable, which can cause distortion and signal loss.

Existing semiconductor backend equipment can be used to execute every step of the process previously described. Thus, a major advantage of MicroCoax is its use of an existing semiconductor manufacturing infrastructure. This is a major motivating factor and advantage behind the potential impact of MicroCoax technology. As previously stated, wirebonding presents a major advantage over flip-chip as it requires very little specialized tooling to address design changes. While the automated wirebonder must be reprogrammed, this can be completed in just a few hours. A redesign in flip-chip can require thousands of dollars in tooling and weeks of non-recurring engineering effort (NRE). MicroCoax preserves the advantages of wirebonding, as it requires only the addition of a simple photomask ($1k in materials and one day leadtime) to realize a design change.

The work that follows describes the simulation, design, fabrication, testing, and evaluation of MicroCoax test structures in order to understand more about their utility and limitations.

3.0 Modelling

CST's Microwave Studio was used to simulate the expected performance of different wirebond test structures. Any I/O structure used to connect to MicroCoax must be compatible with the frequencies over which it was tested. Coplanar probes from GGB Industries were identified as the preferred test interface -- Part# 67A-GSG-150-P for 0-67 GHz and Part# 90-GSG-150 for 55-100 GHz. The geometry of these probes determined the pitch of the coplanar waveguide (CPW) input structure, onto which MicroCoaxes would be mounted. Alumina 5.0 mils thick was the substrate material of choice because it is commonly used for creating passive electrical structures at millimeter-wave (MMW) frequencies.

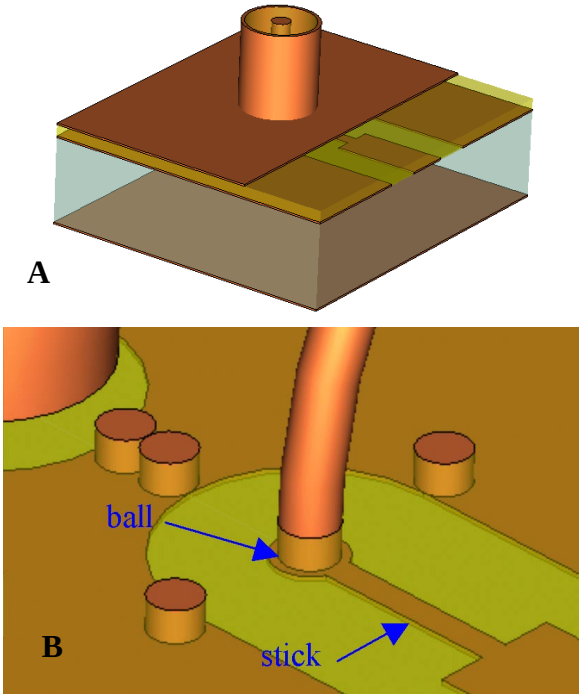

Figure 2, A-B: MicroCoax Input Structure

At MMW frequencies (20-200 GHz), one must pay attention to what are known as mode shapes, or how the electric and magnetic fields relate to one another in a transmission medium. The proper shaping of these fields influences whether or not energy will couple from one kind of transmission line to another. In this case, we coupled a coplanar mode input by our probes, into a MicroCoax, which propagates energy in a TEM (transverse electro-magnetic) mode. The I/O structure, thus, had to be properly shaped to allow the "reshaping" of energy. Modeling was essential to achieve this. One complication was that the wirebond must have a large enough target to which to bond. The input to the coax center conductor, thus, had to have a "stick and ball" type shape to add inductance and achieve the mode match, while also assuring that the wirebond would adhere. Figure 2 shows the input structure with the shield ground in place (A) and with shield ground removed (B) in order to better view the matching structure. Figure 3 shows the ground and signal currents of the CPW input structure. The ground shield and dielectric of the coax have been removed for clarity.

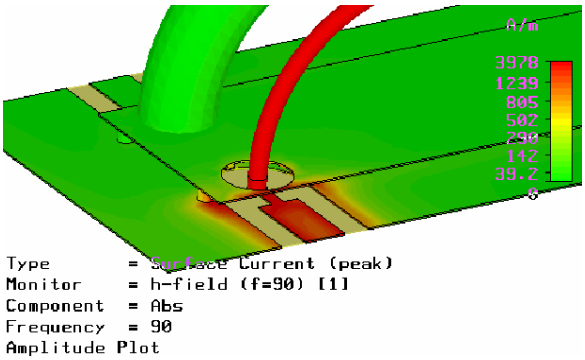

Figure 3: Model Showing Input Structure and Center Conductor Current Distribution

4.0 Design and Fabrication

Two primary performance criteria related to MicroCoax were quantified. The first involved the behavior of single MicroCoax through-lines of different lengths. The second was the isolation of two adjacent lines of differing lengths and spacings. Three different lengths of through-line and six different configurations of isolation structure were implemented, as listed in Table 1. Figure 4 shows a representative isolation structure with dimensions, and the fabricated substrate below it.

Type	Port Distance (mils)	Center Spacing (mils)
Through	21.6, 61.6, 101.6	N/A
Isolation	64 and 80	6.4, 7.4, and 8.4

Table 1: Experimental Substrate Configurations

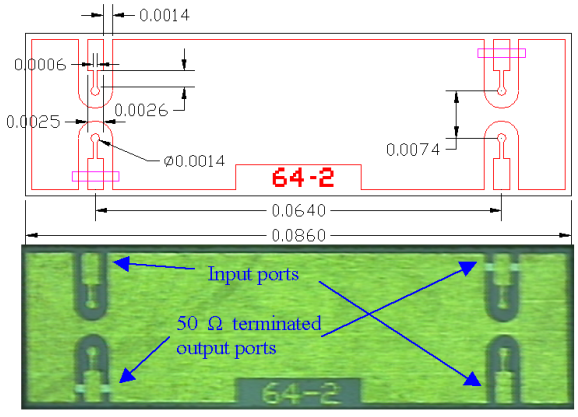

Figure 4: One of Six Different Isolation Evaluation Designs (dimensions in inches)

Note that for the isolation design, there are four ports, two of which have 50Ω terminations. This is because the Agilent 8510C Vector Network Analyzer used for data gathering is a two-port system. Input at the northwest port is terminated at the northeast port. Cross-talk may couple to the adjacent line and appear at the southeast port as a signal on a line terminated at the southwest port. Measurements of coax-to-coax isolation utilize this configuration.

Wirebond diameter was another variable. Test substrates, mounted on Kovar carriers, were wirebonded with two different wire diameters.

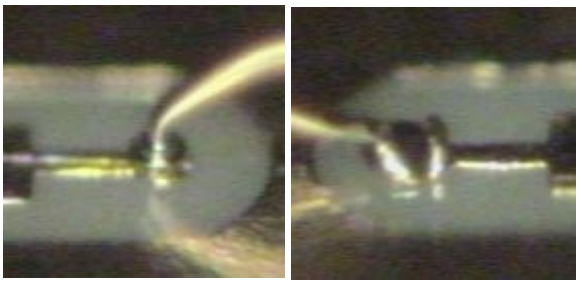

Figure 5-A: 0.6 mil ball bonds

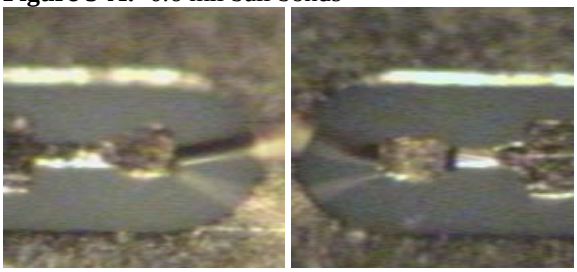

Figure 5-B: 0.7 mil wedge bonds

As coax is a waveguide, performance does not depend significantly on trajectory. Yet wire bond loop shape can play an important role in MicroCoax technology for two reasons. First, to maintain 50 Ω impedance, the ratio of wire diameter to dielectric thickness must be controlled. Larger wire diameter requires thicker dielectric. Therefore, minimizing wire diameter is beneficial. Thinner wire requires better control of looping processes. The ability to shape loops, providing a long flat segment parallel to the substrate surface with a steep descent to second bond, has been available for several years. Thin 0.6 mil wire requires additional control, because of lower wire strength and stiffness. Second, too low take-off angles cause parasitic capacitance to ground at the CPW to MicroCoax transition and can exacerbate thickness non-uniformities for the deposited dielectric and subsequent ground shield layers. Au wire 0.7 mil diameter was wedge bonded using a manual wirebonder, and bonds were individually dressed. A 0.6 mil Au wire was automatically ball-bonded to create stand-off stitch bonds (SSB) using a K&S Maxμm™ *ultra* wire bonder for its advanced looping control. Typical bonds are shown in Figure 5. Note the superior take-off angles for the ball-bonded parts.

The next step in fabrication of the MicroCoaxes was the deposition of dielectric. Parylene C was chosen as the baseline material. Several other candidate films were identified. The criteria for making the final choice were electrical properties, conformality of deposition, deposition rate, and availability. The films listed in Table 2 were evaluated. After some consideration, Parylene N was chosen as the other lead material for evaluation. Teflon would have been very attractive due to its known low loss-tangent, but there were concerns about repeatability of film properties. Dielectric properties for Parylene N and C are not well described in literature above 1 MHz. For this reason, estimations of the dielectric constant (ε_r) and the loss tangent (α) were based on extrapolation from lower frequency data.

Film	**ε_r**	**α**	**Rate**	**Available?**
ParyC	2.73	.013	1.0 μm/hr	Yes. Commonly used in electronic applications
ParyN	2.65	.0006	0.3 μm/hr	Yes. Commonly used in medical applications
ParyD	2.77	.002	---	Not readily Brittle
ParyHT	2.2	---	---	Yes. Only one proprietary supplier; $$$
Teflon	2.0	---	---	Not readily Film conformality not well characterized

Table 2: Conformal Dielectric Films

The following formula [3] is used to estimate the impedance, Z_0, of a coaxial transmission line:

$$Z_0 := \frac{138}{\sqrt{\varepsilon_r}} \cdot \log\left(\frac{b}{a}\right)$$

Where **a** is the diameter of the bond wire, **b** is the outside diameter of the dielectric, and **ε_r** is as indicated from Table 2. From this formula, Table 3 with target values for dielectric thickness was generated:

Film	**ε_r**	**Z_0** (Ω)	**Wire** (mils)	**Dielectric dia** (mils)	**Target dep**(μm)
ParyN	2.65	50	0.7	2.72	25.6
	2.65	50	0.6	2.33	22.0
ParyC	2.73	40	0.7	2.38	18.0
	2.73	50	0.6	2.11	22.6

Table 3: Calculated Film Depositions

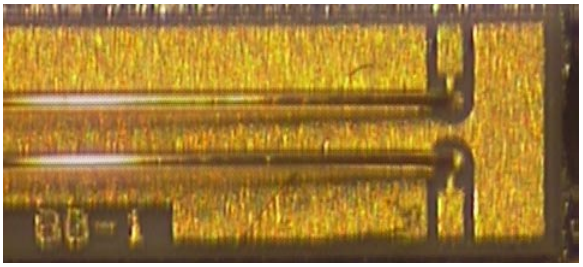

Figure 6: Parylene N Coated Wire Bonds

Once films were deposited (Figure 6), the next step was to perform laser via formation. The laser step had to accomplish two objectives: 1) open up probe pads for electrical test and 2) provide connection between CPW ground and coax shield ground. Several laser approaches were evaluated including a) KrF excimer with mask; b) tripled YAG direct-write; c) quadrupled YAG direct-write. A quadrupled YAG direct-write was chosen based upon availability.

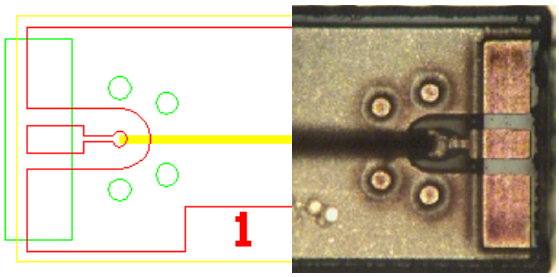

Figure 7: Laser Via Formation Left: green indicates target laser area; Right: lasered I/O region

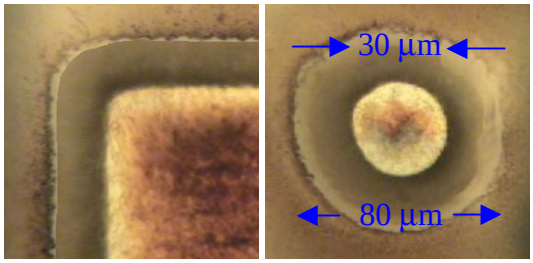

Figure 8: Close-up of Probe Area; Close-up of Via

Figures 7 & 8 show that the laser produced vias with sloped sidewalls (25 µm) for this 26 µm thick Parylene N film. A dark residue is visible on the exposed gold surfaces. This residue, probably carbon compounds from the ablated parylene, must be removed before the Au plating base layer is deposited. The preferred method to do this is to use an oxygen-based plasma, because the residue is not readily soluble in solution. A recipe was developed after optimizing for gas composition, RF power, pressure, and flow rate. Following this are the steps of lithography and plating. These steps, shown in Figure 9, produced excellent results. The final fabrication steps included cleaning the parts of any remaining resist residue and removing the plating base layer over the I/O regions. Completed parts are shown in Figure 10.

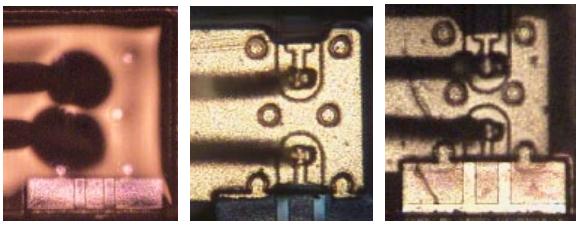

Figure 9: Deposition Steps (Left to right: resist coating; resist pattern & Au plating; resist removal)

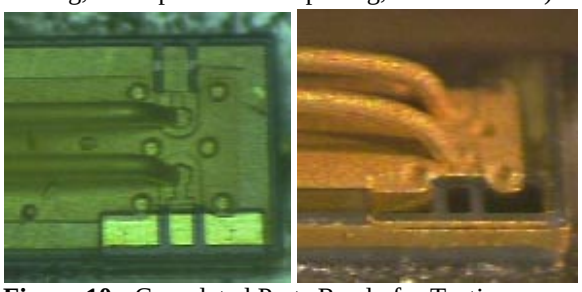

Figure 10: Completed Parts Ready for Testing

5.0 Testing and Evaluation

All part testing was performed using Agilent 8510C Vector Network Analyzer (0-50 GHz) and 8757D Scalar Network Analyzer, in combination with a 4x Frequency Extender from WiseWave (60-90 GHz). Probing was done using a Karl Suss high-frequency device probe station.

Figures 11 and 12 show typical electrical performance of the MicroCoax constructed from 0.6 and 0.7 mil wirebonds, respectively. The loss is slightly better for 0.7 mil than for 0.6, as would be expected from the resistive loss (α) equation below [4], where a and b are the core and dielectric diameters, respectively.

$$\alpha = \sqrt{\frac{\omega \cdot \varepsilon}{8 \cdot \sigma}} \cdot \frac{a + b}{a \cdot b \cdot \ln\left(\frac{b}{a}\right)}$$

σ is conductivity of the metal
ω is the angular frequency
ε is the Parylene dielectric constant

The various "Thru" configurations (D1, D2, D3) had assorted lengths (Table 1) of approximately 22, 62 and 102 mils, respectively. Parylene C and N devices show substantially identical performance for a given device length. The longest samples, ~2.7mm, showed average loss of ~0.75 dB for 55-90 GHz with 0.6 mil core. Estimated performance is graphed in Figure 13. Linear fit is excellent and shows I/O losses of about 0.1 dB and transmission line loss of 0.25 dB/mm. Transmission line loss for 0.7 mil core is about 0.2 dB/mm at 50 GHz.

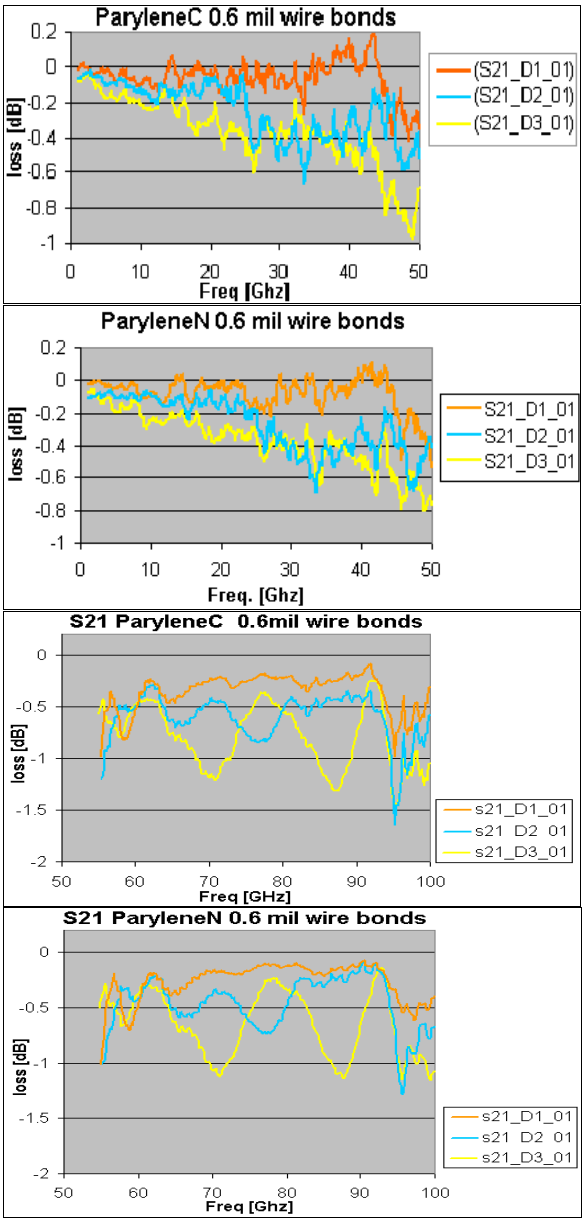

Figure 11: 0.6 mil core MicroCoax Insertion Loss performance (Parylene C&N, 0-50 and 55-100 GHz)

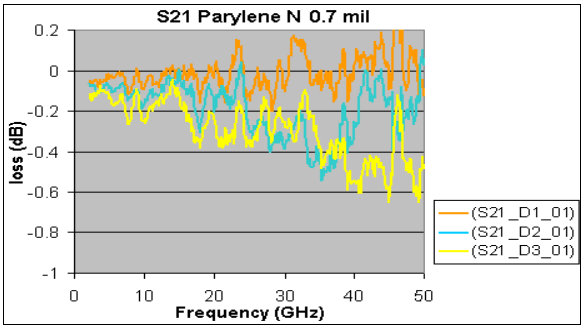

Figure 12: 0.7mil core MicroCoax - 50Ω Impedance

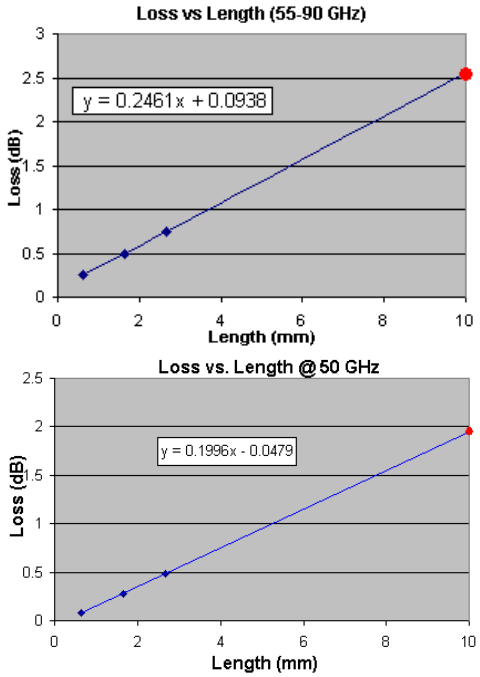

Figure 13: Insertion Loss in 0.6 mil Core (55-90 GHz) and 0.7 mil core (50 GHz)

The ability to limit cross-talk, the level to which nearby signals contaminate one another, is an important advantageous feature of MicroCoax. Test structures were designed to vary the length of lines and the distance between them. Examples of completed structures were shown in Figure 10. Test structures had MicroCoax center-to-center spacings, of 6.4, 7.4, and 8.4 mils. There were initial concerns that dielectric coating and metallic coating uniformity requirements would limit spacing. However, spacing was ultimately limited by the requirement to achieve port-to-port isolation with laser vias, and the impedance match of the input port determining the signal-to-ground spacing of the CPW launch. We expected excellent isolation through the substrate and dielectric layers, as shown in Figure 14. Note that none of the signal on the right-hand port appears at the left-hand port or coax.

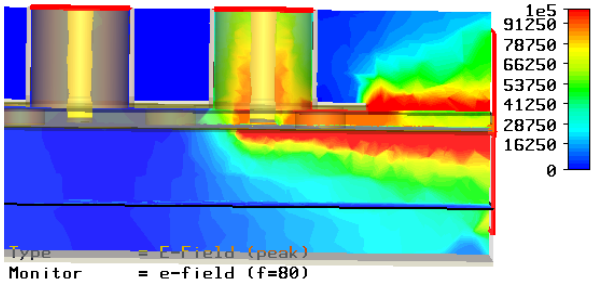

Figure 14: Modeled Isolation Between Adjacent Ports

Observed cross-talk below 20 GHz, was extremely low (<-60 dB), as shown in the graphs of Figure 15. Above 20 GHz, signal begins to appear at the isolation port and grows to a level of about –40dB from about 25-50 GHz. While this is still good isolation, it is not as good as expected.

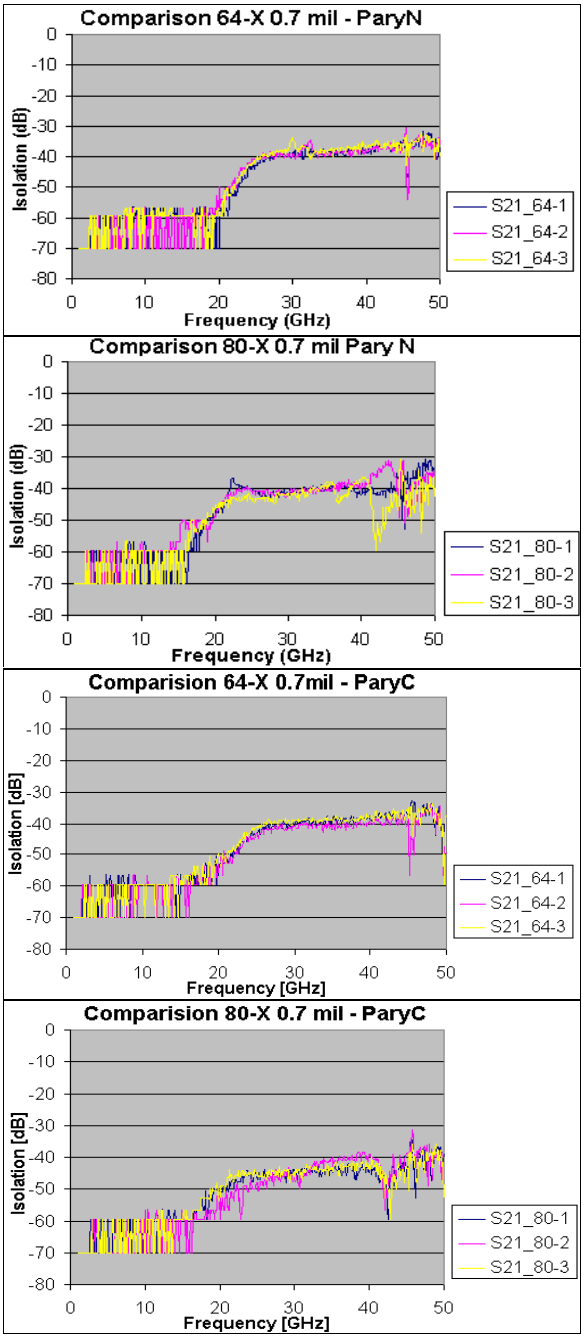

Figure 15: Comparison of Various Cross-talk Structures from 0-50 GHz

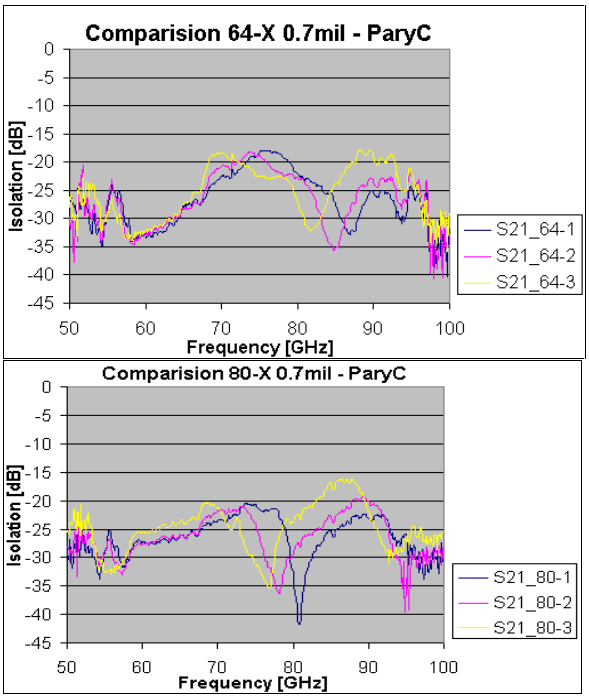

Figure 16: Comparison of Cross-talk Structures from 50-100 GHz

Figure 16 shows generally degrading isolation over the remaining band from 50-100 GHz. In no case is the isolation worse than –15 dB. While results are excellent, they are not nearly as good as expected. An additional interesting observation about Figure 16 is the appearance of notches unique to every substrate design. The position of these notches appears to vary inversely with the volume of the test substrate. This suggests that substrate resonances are present which adversely affect performance. To confirm this, "micro-surgery" was undertaken on the substrates (Figure 17) to see if we could see a change in performance (Figure 18).

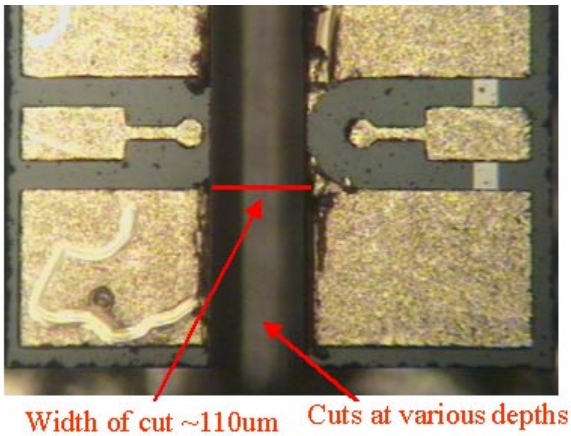

Figure 17: Microsurgery on Isolation Substrate

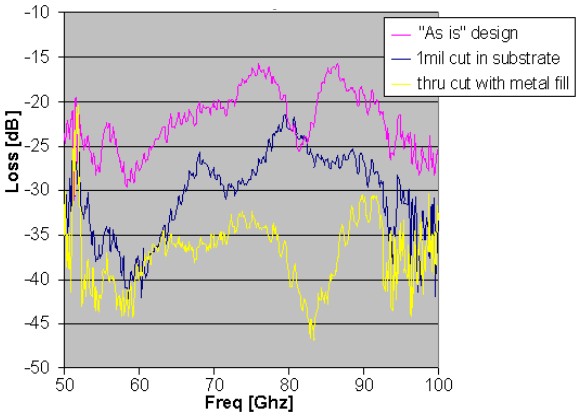

Figure 18: Results of Surgeries (As-is vs. 1 mil cut vs. thru cut with metal fill)

Significant improvement in isolation was seen as a result of cutting the substrate, and refilling it with metal. Since this was not seen in the original model, steps were taken to understand what wrong assumption might have been made in the model construction. After eliminating several possibilities, the boundary conditions of ceramic substrate, which were chosen to be purely radiative, emerged as the primary suspect. The model was reconstructed to include some volume of "air" at the boundaries of the ceramic. The resulting air boundary was made radiative. The model results changed dramatically, showing numerous resonances, as seen in Figure 19.

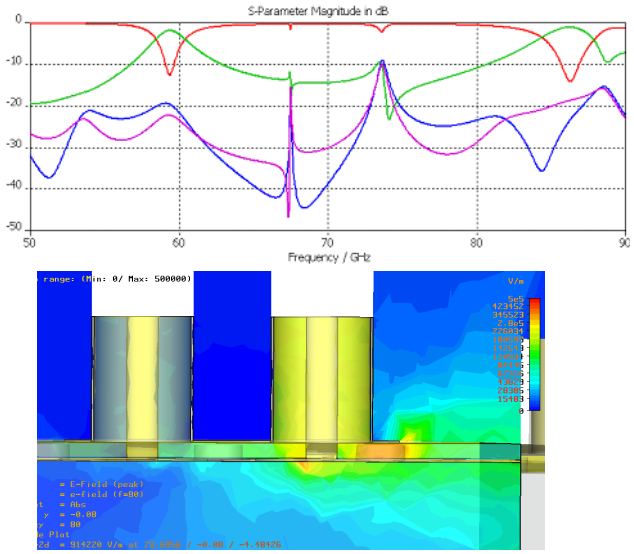

Figure 19: Updated Model Showing Resonances (59, 67, 73, and 86 GHz) and Port-to-port Signal Leakage

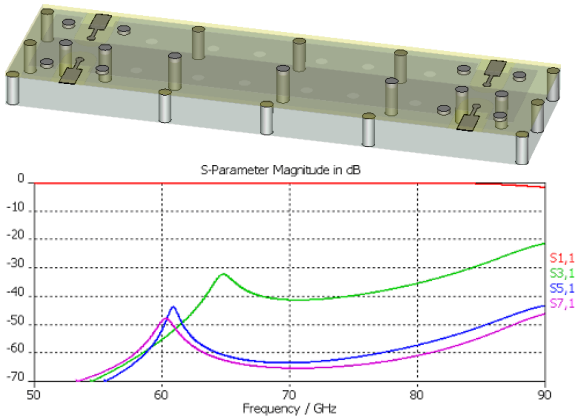

Figure 20: Improved Isolation Design/Model Results

With better understanding of the substrate as the source of cross-talk issues, changes to the design to improve performance were possible. Mostly by adding ground vias around the outside of the substrate, and a few in the bulk, isolation performance was vastly improved. Shown in Figure 20, this is yet to be confirmed experimentally.

6.0 Conclusions

MicroCoax experiments have established the ability to deliver 100+ GHz frequency performance and bandwidth. Prototype devices were designed and manufactured, showing excellent performance over DC-100+ GHz frequency range. Transmission line losses less than 0.5 dB for a typical 2 mm long wire bond, 160 µm pitch, and cross-talk isolation of approximately 40-50 dB from DC-50 GHz were demonstrated. The technology has important implications for improved package design and demonstrates the utility of advanced wire bonding based interconnect approaches.

This work was supported in part by National Science Foundation SBIR Grant DMI-0512916. Thanks to Jim Reed of Optimal Solutions, LLC for his assistance with EM simulation.

References

1) Gordon Moore, "Cramming more components onto integrated circuits", Electronics Magazine, 19 April 1965

2) Luke Collins, "Good Vibrations", Electronic Systems and Software, Aug/Sept 2005

3) Robert E. Collin, "Foundations for MicroWave Engineering" McGraw-Hill, Inc. 1966 , pgs 80-81

4) Ibid, pg. 84