Comparing Flip-Chip and Wire-Bond Interconnection Technologies

Flip-chip assembly and wire bonding are the principal methods for interconnecting ICs. While each offers strong advantages in certain types of applications, packaging is continuing to evolve into a segmented marketplace, with several factors dictating the most appropriate means of interconnection.

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Cost, performance and form factor have become the key drivers in selecting between wire bonding and flip-chip bonding as the "preferred" IC interconnecting method.

Applications such as cellular telecommunications and wearable portable consumer electronics often require the use of flip-chip packaging for its small form factor and, in some cases, high speed.

In other cases, typically with I/Os in the range of 100–600, the existing infrastructure, flexibility and materials/substrate costs of wire bonding provide dominant advantages.

Further segmentation is provided by the emergence of several intermediate hybrid interconnect alternatives, such as stud/ball bumping[1], gold and aluminum ribbon wedge bonding, under-bump metalization (UBM) that can be both bumped and wire bonded, wafer-level packages (WLP) with and without underfill, Direct-Chip Attach (DCA) or CSP packaging. Wire-bonded CSPs take advantage of the existing infrastructure to produce packages with near-chip-size form factors[2].

These alternatives currently are less widely used and will not be addressed in detail in this article.

Figure 1 summarizes the technology choices and associated design issues that typically determine packaging strategy[3]. Cost underlies all initial package choices, and cost reduction pressures continue over a product's lifetime.

Table 1 lists advantages for flip-chip and wire bonding. Many of the advantages depend on the specific application details.

Often, both processes offer advantages. An example is cost. The total cost for a wire-bonded package in the <600-I/O range is typically much less than for an equivalent flip-chip package.

But for a high-volume application, with chips designed and die size minimized to take advantage of flip-chip's efficient use of silicon real estate, wafer cost reductions can significantly lower the total cost per flip-chip package below that of the comparable wire bonded package.

Advantages

In general, the flexibility, infrastructure and cost of wire bonding are its major advantages. Package size is smaller, and device speed is normally higher for flip-chip. System speeds with wire-bonded packages designed for high signal-propagation rates (e.g., RDRAM, BOC), however, remain competitive[4]. Flip-chip devices often have many more bumps than equivalent wire-bonded devices have bond pads.

Because the bumping cost/wafer is fixed (independent of how many bumps there are per wafer), there are electrical advantages to designing in additional bumps. As chip

voltages drop and current requirements increase, it is advantageous to distribute power and ground directly to the core of the devices, with area array solder bumps to minimize voltage drop.

These low-inductance power and ground paths also minimize SSN (simultaneous switching noise) and ground bounce. On especially sensitive signal paths, additional power and ground bumps can be used to surround the sensitive I/O bump, shielding the bump from noise induced by neighboring circuitry.

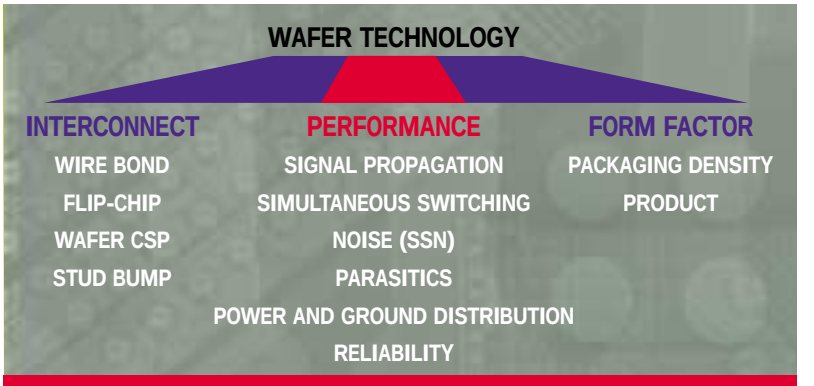


FIGURE 1: TECHNOLOGY CHOICES

Process Descriptions

Table 2 shows process flow for both flip-chip and wire bonding on an organic substrate.

For flip-chip wafers that were originally designed with peripheral pad layouts for wire bonding, more steps are added. The wafer-bumping stage includes redistribution of the peripheral bond pads to an area array design.

Dielectric and metal layers are added to redistribute and connect the aluminum bond pads to area array bumps.

The Differences

The two processes are substantially different from an automation perspective. Wire bonding is best characterized as a single-point-unit operation. Each bond is individually produced.

Die on their carrier or substrate are moved through a wire bonder. The machine's pattern recognition system identifies the die, transforms and corrects the taught locations for each bond, and individually moves to each location to produce an interconnection.

Flip-chip is a wafer-scale operation. Bumps are formed on an entire wafer, and the wafer is diced; individual die are picked, fluxed and placed on the substrate.

The flux must be tacky enough to hold the die in place for handling through reflow. The solder is reflowed above its melting point to form the interconnection. Underfill and encapsulation processes complete the assembly. At all times, the process handles entire wafers, die or substrates. It is never a single-point operation.

Ultra-CSP

WLPs, such as the Flip Chip Technologies' Ultra-CSP shown in Figure 2, are CSPs that are processed at the wafer level. The WLP opens up new CSP applications in both low-I/O-count packages and those that require very small form factors. In most applications, the Ultra-CSP does not require underfill, providing additional opportunities for cost reduction.

TECHNICAL BENEFITS

Technology Thresholds

Current leading-edge flip-chip designs are in production with as many as 5,908 bumps/chip at 200-µm pitch and 1,500 bumps/chip at 170-µm pitch in area array configurations.

TABLE 1: PROCESS ADVANTAGES

WIRE BOND
- FLEXIBILITY
- INFRASTRUCTURE
- COST
- RELIABILITY

FLIP-CHIP
- DEVICE SPEED
- POWER AND GROUND DISTRIBUTION
- I/O DENSITY WITH AREA ARRAY
- PACKAGE SIZE/FORM FACTOR
- LOW STRESS OVER ACTIVE AREA
- RELIABILITY

TABLE 2: ASSEMBLY PROCESS COMPARISON ON ORGANIC SUBSTRATE

WIRE BOND	FLIP-CHIP
• WAFER	• WAFER
• DICE	• WAFER BUMPING
• DIE ATTACH	• DICE
• CURE	• PICK AND PLACE PLUS FLUX
• WIRE BONDING	• REFLOW
• ENCAPSULATE	• UNDERFILL ENCAPSULATION
• BALL ATTACH	• BALL ATTACH
• MARK	• MARK
• SYSTEM TEST	• SYSTEM TEST

Figure 3 shows a high I/O-flip-chip device at 178-µm pitch full area array. Future production area array pitches will continue to reduce to 150-µm in the next two years and eventually to the 100-125-µm range as the substrate technology becomes cost effective. The rate of pitch reduction is likely to moderate as design tools become available to take full advantage of the area array capabilities of flip-chip technology.

Current mass production for wire bonding is in the 60-µm range, and a production capability of 50-µm is believed to represent the leading edge in wire bonding.

Figure 4 shows development results for very fine 35-µm pitch wire bonds. Wire bonding technology in this range is feasible, and equipment that will allow manufacturers to reach this threshold is under development.

Getting the Lead Out

An inherent advantage of thermosonic/ultrasonic bonding is that there is a true weld, joining the two metals through an inter-metallic phase.

Conversely, all flip-chip devices use solder interconnects, formulated in two, three- and four-part (binary, ternary and quaternary) alloys. Solder is a metallic alloy with a low melting point.

The solder melts (reflows) and the liquid phase wets the two metals that are joined. When the solder solidifies, it provides a mechanically strong joint with low electrical resistance. The best solder alloys for flip-chip applications are the Sn/Ag/Cu alloy systems, with the possible inclusion of an additional element. A solder bumping technology, such as solder paste, is preferred over plating to achieve the control of the elements in the alloy as bumped.

Typical electrical solders contain lead—this is expected to change as lead-free alloys are introduced. Lead-free telecommunications devices will be on the market this year.

Green marketing is the primary driver for the development and commercialization of lead-free solder technology. Once the first device marketed and advertised with lead-free logos and designated as environmentally friendly enters the marketplace, it will be a primary qualifier for an OEM in doing business.

Ternary and quaternary lead-free solder alloys will be the primary choices for these products.

An additional benefit of lead-free alloy systems is that they have the potential to minimize the soft errors produced by lead alloys.

These errors are caused by alpha particle emissions from radioactive isotopes common in Pb-based alloys.

In Japan, many OEMs will specify lead-free to meet upcoming legal requirements. In Europe and the U.S., the telecom market will demand this feature as a basis for conducting business.

Reliability

Flip-chip processes include fluxing, placement and reflow, as well as the underfill material and dispensing processes. Underfill is normally required for flip-chip devices on laminate substrates to eliminate solder fatigue.

This fatigue is caused by cyclic strain resulting from a TCE mismatch between the chip and the substrate during thermal cycling. The underfill must be stiff enough to restrain the large expansion/contraction of the laminate and reduce the strain on the solder bump. A well-characterized flip-chip assembly process can achieve high yields and reliability.

Fine-pitch wire bonding is also a complicated process. Molding fine-pitch wire bonds requires additional process capabilities to avoid wire sweep and deflection.

Finer diameter wires, required to achieve fine pitch are not as strong or as stiff as larger diameter wires. To address these constraints, manufacturers are developing higher strength wire alloys, copper-wire bonding and encapsulant formulations to minimize sweep at fine pitches and with long wires.

Through process integration, additional supplier support, and improved equipment and materials capabilities, fine-pitch wire bonding also can achieve high yields and reliability.

FIGURE 2: *ULTRA*-CSP

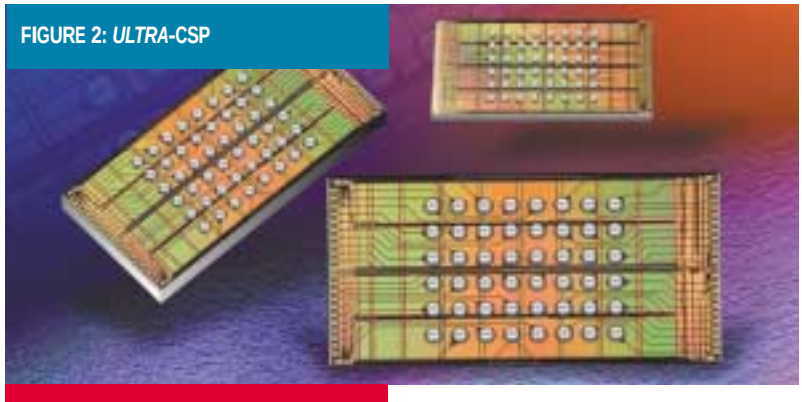
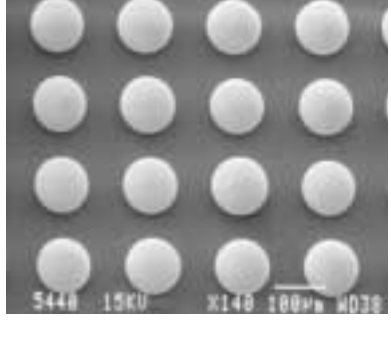


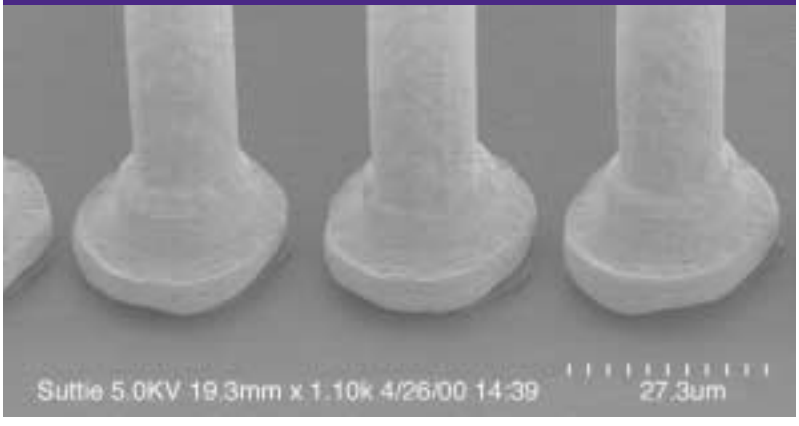
FIGURE 3: HIGH I/O



Cost Analysis

Cost comparisons and analyses are highly dependent on modeling conditions and, in particular, are sensitive to the choice of substrate technology. Optimum substrate choices often change through the life of a

FIGURE 4: FINE-PITCH WIRE BONDS



product, depending on production volume, substrate layers, microvias[5] vs. conventional multilayer, among other considerations.

Technical reasons requiring flip-chip's electrical performance or form factor are usually the most important criteria for a change from wire bonding to flip chip.

Wafers designed specifically for area array flip-chip may have smaller die, because peripheral bond-pad layout (in pad-limited devices) requires a larger die perimeter to escape the required I/O. Die size is a dominant factor in the cost of a chip and represents a significant advantage for flip-chip.

This advantage however, may be reduced, because the additional substrate density, required to escape the area array flip-chip bumps may be more costly and require additional substrate layers or microvia technology.

High-Speed Packages

Three years ago the SIA roadmap[6] and other sources predicted that the speed required for new devices would soon exceed the capabilities of wire bonding and that flip-chip would be the interconnection method able to meet the speed requirements of advanced packaging.

Today, the same prediction can be made, but the edge of the envelope has been redefined. RAMBUS' RDRAM and board-on-chip packaging is being produced with wire-bonded interconnections operating at speeds of 400 MHz, which were not considered feasible only a few years ago.

Wire-bonded RF packages with speeds of 2.4 GHz are available today. Future packaging designs, with short wire lengths and very fine bond pitch, will continue to push out the edge of the envelope for the foreseeable future.

Flip-chip still has a technology advantage, but wire bonding remains highly competitive.

The Future

Both wire bonding and flip-chip will continue to coexist as growth technologies into the foreseeable future, and the IC packaging market will remain a continuum of technology choices.

Where flip-chip is advantageous, it will be the production method. As the flip-chip infrastructure is established, costs will be reduced and the application space will broaden.

Where applications can be produced by wire bonding, its cost advantages will determine the interconnect method.

New technologies, such as WLP, WLBI (wafer-level burn-in), stacked packages and optical interconnects, as well as incremental advances in current technologies—such as flip-chip and wire bonding—will continue to redefine the continuum of product and process solutions for the interconnection of the die to the external world.

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