Gold Stud Bumped Flip Chip: Surface Mounting and Joint Integrity with Thermal cycling

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Abstract

The developing portable electronics market continues to fuel the demand for smaller, lighter, better performing, low cost components. This trend will continue as each new generation of cellular phones, laptops, personal digital assistants (PDA) and smart labels demands new features and enhanced performance. The assembly technology of flip-chip has been an excellent low cost, high performance solution for many of these applications. Flip Chip Bump Packaging (FCBP) has seen an explosive growth in recent years. This paper discusses the processing of the gold bumps, various conductive adhesives used during the interconnection of the bumps and the factors influencing the joint integrity and the thermal cycling of the gold bumps.

1.0 Introduction

Microelectronics device packaging is undergoing major changes driven by technical, business, and economic factors. From the traditional role of a protective mechanical enclosure, the modern microdevice packaging has been transformed into a sophisticated thermal and electrical management platform. Recent advances in microelectronics packaging indicate a migration from wire bond (where the chip or die is interconnected to the package only on the periphery of the die) to flip-chip (where the die is interconnected to the package using the entire die area); and from ceramic to organic packages, with various technologies emerging as key form-factors. The bump technology will solve the manufacturers problem for any applications requiring high performance, smaller and faster electronics.Stud bumping requires no under-bump metallization (UBM). The advantage of the bump interconnect solution is the reduced interconnect length which reduces power consumption and lowers the inductance and signal loss. By using the chip interconnect process; the IC can be electrically connected in a compact fashion. Flip chip technology is very suitable for light and real chip size packaging. The concept of flip-chip process where the semiconductor chip is assembled face down onto circuit board is ideal for size considerations, because there is no extra area needed for contacting on the sides of the component. The performance of flip chip technology in high frequency applications is superior to other interconnection methods, because the length of the connection path is minimized. Also reliability is better than with packaged components due to decreased number of connections. In flip-chip joining there is only one level of connections between the chip and the circuit board.

2.0 Migration from Wire Bonding to Flip Chip

Wire bonding was the most common die connection technology in themicroelectronics industry. The die is faced up and mounted down using various epoxies and metals to the substrate. The three processes of wirebonding are ultrasonic bonding, thermocompression bonding and thermosonic bonding. Among all, thermocompression bonding is the earliest technique used and the other types of wire bonding were introduced when low temperature was required by thermally sensitive devices [1].

The biggest advantage of wire bonding is its process flexibility and the sheer quantity of wire bonders in use today. As a consequence, it is a mature technology and the production process is thoroughly researched and well understood. New package designs and tighter control of wire length in high frequency applications have further expanded the electrical performance range of wire bonded packages.

The main disadvantage of wire bonding is that the number of bonds is proportional to square root of die area due to which it is not great for distributing large amounts of power and for large numbers of I/O's. High speed machines bond several wires per second. But as the need for smaller packages grow, more wires were needed which lead to problems. As the wires at the periphery of the die are closer together, there are more technical issues including electromagnetic interference, they create [2]. A better technology, flip chip technology is introduced in order to overcome the power requirements and to promote thinner packaging.

In the Flip Chip assembly, the electronic components are flipped and attached on to the substrates, circuit boards or carriers, by means of conductive bumps on the chip bond pads [3]. The bumps in the flip chip technology make all the required electrical, mechanical and thermal connections to the substrates. The main advantage in the Flip Chip technology is lesser interconnection length when compared to wire bonding due to which there is significant signal inductance reduction. The reliability issues on Flip Chip are quite different from the previous technology namely wirebonding where yields and manufacturing defect were predominant [4]. The bump geometry plays a very important role in distributing the applied strains throughout the material.

3.0 Electrically Conductive Adhesives in Flip Chip Technology

Conductive adhesive joining in the flip chip packaging offers the potential for low cost, high reliability and simpler processing. There are two kinds of conductive adhesives. They are Isotropically conductive adhesives (ICA) and Anisotropically conductive adhesives (ACA). The conductive adhesives are compatible with a wide range of surfaces including non-solderable ones. The major advantage is that they have finer pitch capability [5]. Conductive adhesives are classified based on the direction they conduct and also by the difference in their polymer structure.

3.1 Isotropic Conductive Adhesives

Isotropically conductive adhesives are pastes of polymer resin that are filled with 25-35 volume percent of the conductive particles. Since these adhesives have the conductive particles in all directions, they conduct in all directions. These offer a low processing temperature solution. ICA's have poorer high-frequency performance compared to metallic solders.

3.2 Anisotropically Conductive Adhesives

Anisotropically conductive adhesives are pastes or films of thermoplastics or b-stage epoxies. They are filled with metal particles or metal coated polymer spheres to a content that assures electrical insulation in all directions before bonding. These adhesives contains about 5-10 volume percent of the conductive particles. After bonding the adhesive becomes electrically conductive in z-direction. The metal particles are typically nickel or gold and these metals are also used to coat polymer spheres. ACA becomes conductive only when it is compressed thermally during the bonding. When the adhesive is compressed, the conductive particles align themselves in z-direction between the connecting bumps and pads forming a conduction path only in that direction. At this stage, the insulation layer of the conductive particles wears out and electrical connections are formed in the z-direction. . The other conductive particles remain as usual with the insulation layer and prevent electrical conduction in the x and y directions [6]. The below figure shows the alignment of the conductive particles during ACA bonding.

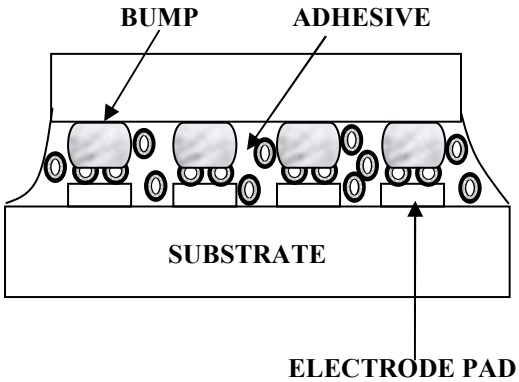

Figure 1: ACA Bonding

The ACA joints have the same high-frequency performance up to 20GHz frequency. But the major loss is on the substrate that it is probably not suitable for use due to large losses [7]. The conductive particles of the film form adhesive are gold plated metal nucleus corpuscles and the paste form of the adhesive has the gold plated plastic nucleus corpuscles conductive particles.

The limitation of the adhesives is that they do not self align and hence higher placement accuracy is necessary compared to solder. ACA bonding needs pressure undercure which implies that the conventional reflow process cannot be used for curing. Hence, special bonding equipment is needed.

Generally, humid conditions cause most reliability problems with adhesive flip chip joints [12]. Typical failure mechanisms are caused by diffusion of water molecules into adhesive layer as well as into the interface between substrate and adhesive. This causes an irreversible decrease of mechanical and adhesive strength, a reversible increase of plasticity, a decrease of glass transition temperature and swelling. There was a lot of research done on the use of conductive adhesives in the gold stud bumping.

4.0 Flip Chip Technology

In 1960's the solder bump interconnection technology was a replacement to the traditional wirebonding. A solution for the expensive, unreliable and low productivity WB process was needed. The demand for more functionality and reliability of the ever increasing I/O count lead to the flip chip technology.

The flipchip technology will make the die become a stand-alone package. Protection of this new package would become a challenge, and under bump metallurgy (UBM) discipline is no more. The active devices in the die will now face the connections, i.e., the die needed to be flipped.[1].A great advantage of the reflowable bump technology is its self-alignment capabilities from the high surface tension of the materials involved.

The three stages in making flip chip assemblies are: bumping the die or wafer, attaching the bumped die to the board or substrate, and, in most cases, filling the remaining space under the die with an electrically non-conductive material. The conductive bump, the attachment materials, and the processes used differentiate the various kinds of flip chip assemblies. The most common bumping and attaching methods are the solder bump flip chip, plated bump flip chip, stud bump flip chip. The attachment of high I/O devices becomes very cost competitive in flip-chip, compared to conventional die and wire bonding technology, since thousands of I/Os can be connected in a single process step[9].

The reliability issues on FC are quite different from the previous technology namely wire bonding where yields and manufacturing defect were predominant. FC technology must survive strains imparted by mismatch in expansion of the die and the die carrier. These displacement mismatches arise from different coefficient of expansion (CTE), temperature excursions and temperature gradients the package experience during regular operation. Such displacement mismatch increases with the size of the package. In general, bumps further away from the centroid of the package, will have higher strain and hence shorter life [4].

Flip chip assembly has significant advantages over other microelectronic packaging. One can choose from several varieties of flip chip bumps including solder bump, plated bump and stud bump. The application, cost, under-bump metallization, and underfill all contribute to choosing the best suited flip chip bump [10]. The other advantages of flip chip technology are its smaller size, increased functionality, improved performance, better high-speed routing, less inductance, resistance and capacitance, smaller electrical delays (shorter distances from the circuit to the bump), good high-frequency characteristics and improved reliability.

However, for some cases during actual power on/off cycling, where high temperature gradients may be present, buckling can cause interior bumps to experience highest strains and consequently shorter cycle fatigue life. The bump geometry for nonencapsulated packages plays a very important role in distributing the applied strains throughout the material. The height of the bump plays a key role in fatigue life, a quadratic relation exist

between bump height and fatigue endurance. The average strain of a bump is inversely proportional to tits height, and the work done by the interconnection can be derived to be a quadratic function of the strain.

4.1 Solder Bump Flip chip

The first step in solder bumping includes cleaning, removing insulating oxides, and providing a pad metallurgy that will protect the IC while making a good mechanical and electrical connection to the solder bump and the board [11]. Under bump metallization (UBM) consists of successive layers of metal layers under the solder bump which is indispensable for reliable flip chip interconnection. The various metal layers in this process are: adhesion layer, diffusion barrier layer, solders wettable layer and a protective layer.

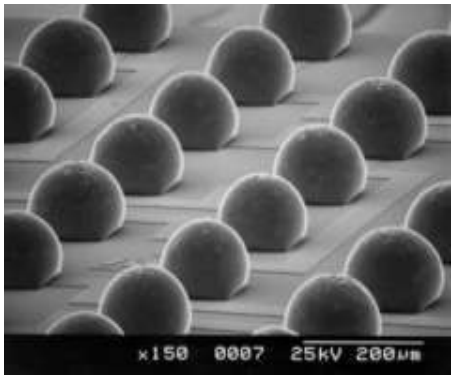

Figure 2: Solder Bumps

The different methods for producing solder bumps are through evaporation, plating, printing, stud bumping, direct placement and jetting. The solder bump chip is flipped and joined to a corresponding array of lands on the substrate. Tacky flux is applied to the solder contact areas either by dipping the chip into a flux reservoir or by dispensing flux onto the substrate. For coarse pitch applications (>0.4 mm) solder paste is deposited on the substrate by stencil printing [12]. The steps of flipchip soldering process are: die preparing (testing, bumping, dicing), substrate preparing (flux application or solder paste printing), pick, alignment and place, reflow soldering, cleaning of flux residues (optional), underfill dispensing, underfill curing.

The advantage of solder bumping over wire bonding is its ability to use the majority of the chip surface for interconnect pad sites and can utilize an array pattern across the face of the chip, allowing many more interconnect locations. The flexibility of interconnections allow the optimized chip designs because signals can be routed out almost anywhere on the chip due to which the size of the chip is reduced and the performance of the chip is improved by reducing resistance and capacitance [13].

The main disadvantage of the solder bumping is that, this is applicable only at the wafer level but not at the single die level. This led to various solutions such as gold bump solution, copper bumps, and conductive-epoxy bump connections [12].

4.2 Gold Stud Bumps

Gold stud bumping is done by modifying the traditional wire bonding technique. This is a sequential process where the bonder produces bumps individually. The resistivity of gold is lesser than leaded and lead-free solder alloys, providing better current carrying capacity. The thermal conductivity of gold is superior to solder and this causes better heat transfer [14].

4.2.1 Process of Gold Bumping

There are two steps in the process of forming gold stud bumps: bumping and coining. Bumping is a process where a normal ball bond with a short protruding ductile fracture tip from the top of the ball is bonded to the device and then coined flat by a second stage operation. Bumping is similar to the wire bonding except that the wire bonder must have suitable software to handle bumping process. Due to this the bond cycle time is improved and all the unnecessary motions of the wire bonding are eliminated in this process [15]. During the motion of the wire bonder, the wire will break at the length of the Heat Affected Zone (HAZ), which is the recystallized segment of the wire directly above the ball. The gold wire is alloyed with 1% Pd to abate the breaking of wire above the bump. During the bump formation the wafer/substrate must be heated to 150- 200°C. The height of the tail formed on the bump depends on the length of the Heat Affected Zone. The variability in the length of the Heat Affected Zone will result in the formation of non uniform balls. The better control on the Heat Affected Zone (HAZ) is the key factor in forming the uniform balls. The height of the bump formed also depends on the diameter of the wire used to form the bump. The

gold bump formed with the tail is the Standard Bump. But the main drawback with this kind of bumps is the variability in the diameter of the bumps. Hence a second step is usually performed for a better control in the height and diameter of the bumps. The second step in forming the gold bumps is "coining". Coining is a process where the stud bumps can be flattened or coined by mechanical pressure to give a flat top surface and uniform bump heights as well as flattening any remaining wire tail. The flat surface thus formed on the gold bump defines the conduction path of the bump. The figures below show a gold bump with a tail and a bump after coining.

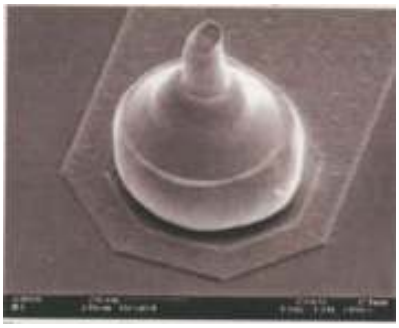

Figure 3: Gold bump with a tail

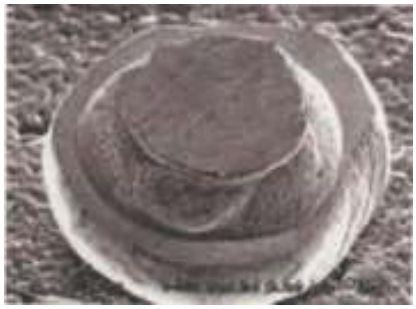

Figure 4: Gold bump after coining

Gold bumps require low temperature process when using adhesive joining and they also have high interconnection density at chip periphery compared to wire bond. Using gold bumps results in thin lightweight packages. Gold bumps have superior performance in radio frequency (>1GHz) when compared to solder bumps. Electroplated gold bumps are used for chip on glass interconnection of LCD drivers using anisotropic conductive adhesives to make the electrical and mechanical joint between IC and LCD. Solder bumps cannot be used in such applications because of the need for high temperature for solder reflow and LCD cannot withstand such high temperature [16]. The disadvantage is that gold bumps are not compatible with surface mount assembly.

The used materials not the technology govern the environmental issues, such as material handling and waste disposal. The use of flip chip joining has been, however, encouraged with external environmental arguments [12]. With flip chip technology the size of the manufactured devices is decreased which cuts down the use of raw materials. Nevertheless, companies do not change to flip chip technology for purely environmental reasons. The environmental arguments can motivate the use of adhesives in flip chip joining, because adhesives generally provide a lead free alternative.

4.2.2 Joint Integrity of the Gold Bumps

The various factors affecting the bump joints are the size and shape of the bump, pad size, size of the conductive particles of the adhesive and temperature. Along with the planarity of the bump, all the conductive particles of the adhesive should deform uniformly during bonding in order to obtain a reliable joint with respect to different environmental tests [7].

Many studies showed that the variation in the size of the bump or pad having the uniform conductive particle size also results in a bad joint under either high or low temperature ranges. The variation in the size of the conductive particles causes failure with different temperature changes. The non-flat surface on the substrate and the large variation in the bump height across the die can cause poor bond quality due to uneven pressure distribution and this will cause electrical opens at both low and high temperatures. Pressure distribution during bonding causes uneven deformation of the conductive particles. The pad size has an effect on the electrical conductivity in a joint since a large pad allows more particles to stay on the pad [7]. The critical factors determining the reliability of thermocompression bonded chips is similar to bonding with solder joints, such as the difference of TCEs between the chip and the substrate, the height of joints and the maximum distance between joints. It is likely that most of the damages (cracks) to the bond area are created during the cooling from the high bonding temperature. The susceptibility to fatique damage of gold is much lower than that of solder due to its much higher melting temperature, so if the adhesion strengths between the bump and the pads are not exceeded during thermal cycles the reliability would not be a problem [12]. The

underfill material used between chip and substrate increases drastically the reliability of the joints for thermal fatigue. Thermal fatigue of joints is an important reliability issue for flip chip joinings where no underfill material is used.

4.2.3 Thermal Cycling

Thermal cycling from -40 to +125°C, 1000 cycles with a certain amount of dwell time and transit time is one of the standard reliability tests for the gold stud bumping. Stress/strain developed during the bonding can be analyzed using this test. The bumped die connected to a suitable substrate is undergone about 1000 thermal cycles and the structure of the bumps, strain on the bumps are analyzed. The deformation of the bump can be studied by the finite element analysis of the gold stud bumped die. If a low height is seen in the bumps then there is a reliability problem for the substrate as there is increase in the electrical resistance of the daisy chains. Extremely bump height also causes a reliability problem due to porosity formation. The below figure shows the deformation in the bump due to the extreme bump height.

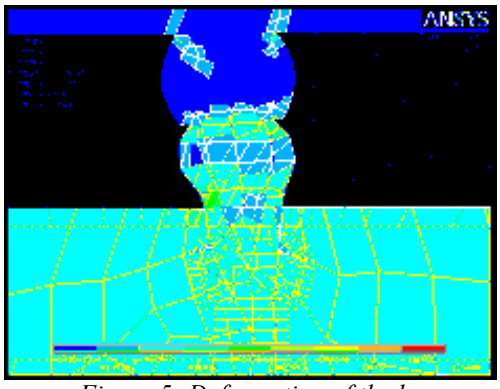

Figure 5: Deformation of the bump

Applications

Flip Chip Bump Packaging (FCBP) has seen an explosive growth in recent years. Over billion devices are now assembled using this technique. The majority are low lead devices such as liquid crystal display drivers, watch modules, smart cards and many other such highly efficient and economically feasible devices.

Chip-On-Glass is one of the mounting methods that uses gold bumps and is used in most compact applications [16]. This technology reduces the mounting area and is better suited to handling high-frequency or high speed signals and also gives a near turn solution for lower cost, higher performance, compact and light weight systems. By using this technology, the displays are brighter, long lasting and require less power than conventional VFDs (Vaccum Flourescent Displays). Adhesives used in the Chip-On-Glass technology are the anisotropic conductive adhesives (ACA).

Conclusion

The migration from wirebonding to flip chip technology led to a compact packaging with good performance. The use of gold bumps have high yield compared to solder bumps. The use of anisotropic conductive adhesive for the interconnection avoids the underfilling step which comes under the economical and time issues. Various experiments are being conducted to reduce the diameter and the height of the gold bump. All these factors put together leads to more efficient and economical package. Recent advances in bumping will enable more compact packaging to meet the demands of the manufacturer both economically and technically.

References

[1] Horatio Quinones, Alec Babiarz, "Flip chip, CSP and WLP technologies: A Reliability perspective",Asymteck Headquarters Carlsbad CA, USA. IMAPS Nordic, sept 2001.

[2] Paul Sibler ud," Essential education for wafer-level packaging", SECAP(semiconductor equipment consortium for advanced packaging), semicool, Kalispell, mount EP&P, Jan 2001

[3] George A. Riley " Introduction to flipchip: what, why, how", www.flipchips.com, oct 2000.

[4] Dr. Thomas Tschan, " Deciding between flipchip and wire bonding", ESEC Switzerland.

[5] Johan Lin, Zanghie Lai, "Reliability of Anisotropically conductive adhesive joints on a flip chip/ FR-4 substrate", Journal of Electronic packaging, Sep 2002, vol.124 pg 240- pg 245.

[6] "A continuous contact resistance monitoring during the temperature ramp of anisotropic conductive adhesives film joint", journal of electronic materials, jan 2004.

[7] J Liu, "Recent advances in conductive adhesives", Microsystems technologies(1998) pg. 72.80.

[8] H. Nishida, K.Sakamoto, Hideki Ogawa and Hiromi Ogawa, " Micropitch connection using anistropic conductive materials for device IC attachments to a liquid crystal display", IBM

jounal of Research and Development, Vol 42, nos 314, 1998 High Resolution Display.
[9] Dr. Thomas Tschan," An overview of flip chip technology", ESEC, Switzerland.
[10] George A. Riley, tutorials #1, www.flipchips.com
[11] George A. Riley," Solder bump flipchip" www.flipchip.com
[12] Nordic Electronics Packaging guideline.
[13] John Franka, Kathy Glessner, David wontor, "Solder bump technology: present and future", Advanced packaging technology, Motorola semiconductor products sector, Austin, Texas, USA.
[14] Vince Mc Jaggart, Lee Levine and gene Dunn, "Stud bumping and die attach for expamded flipchip application", Advanced packaging, sep 2004.
[15] Lee Levine," Ball bumping and coining operations for TAB and flipchip", Kulicke & Soffa Industries, Inc.
[16] Jorg Jasper," Gold or solder chip bumping, the choice is application dependent", EM-Marin.